FIG. 1

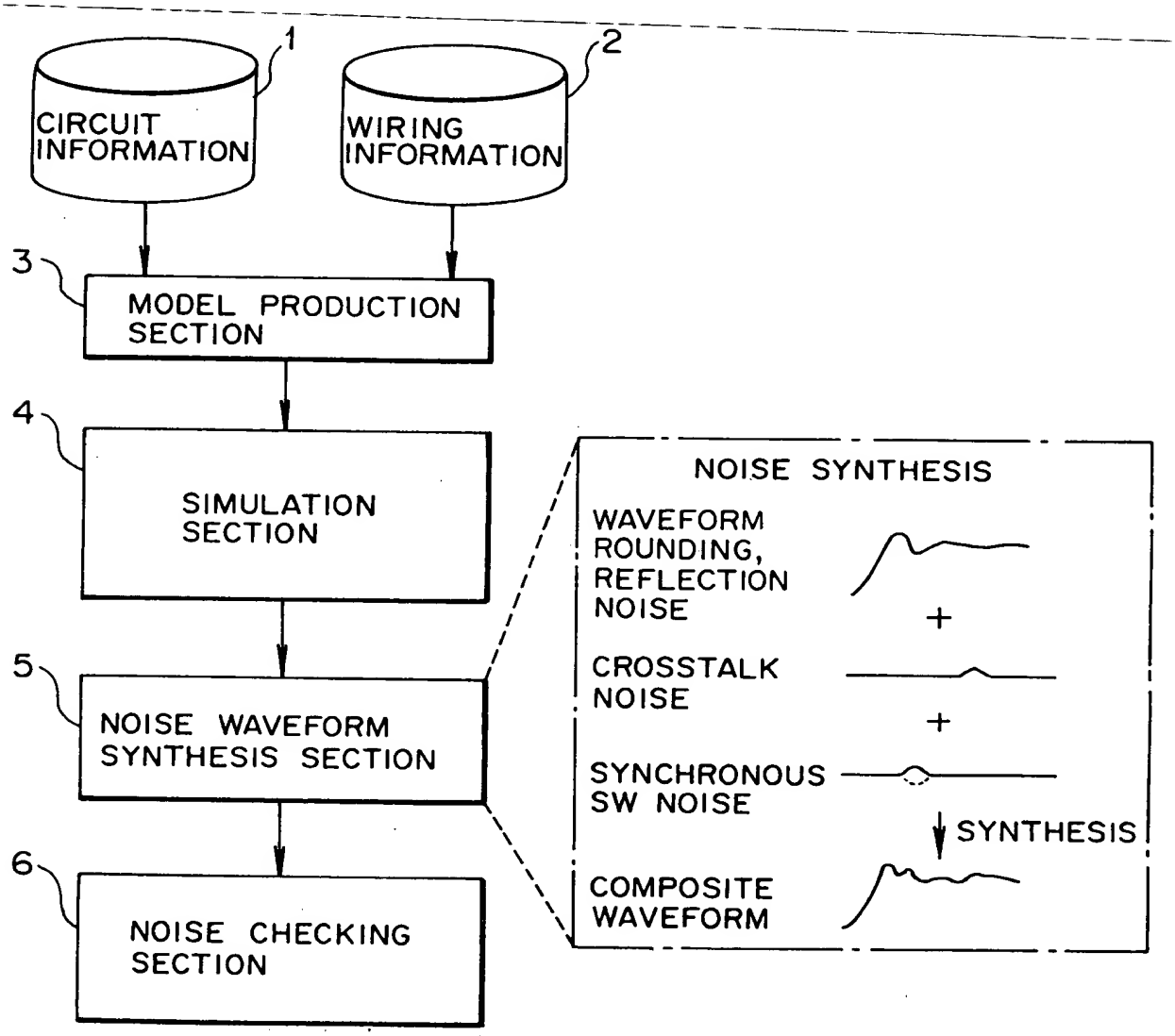

1
CIRCUIT INFORMATION
2
WIRING INFORMATION
3
MODEL PRODUCTION SECTION
4
SIMULATION SECTION
5
NOISE WAVEFORM SYNTHESIS SECTION
6
NOISE CHECKING SECTION
NOISE SYNTHESIS
WAVEFORM ROUNDING, REFLECTION NOISE
+
CROSSTALK NOISE
+
SYNCHRONOUS SW NOISE
SYNTHESIS
COMPOSITE WAVEFORM

FIG.2

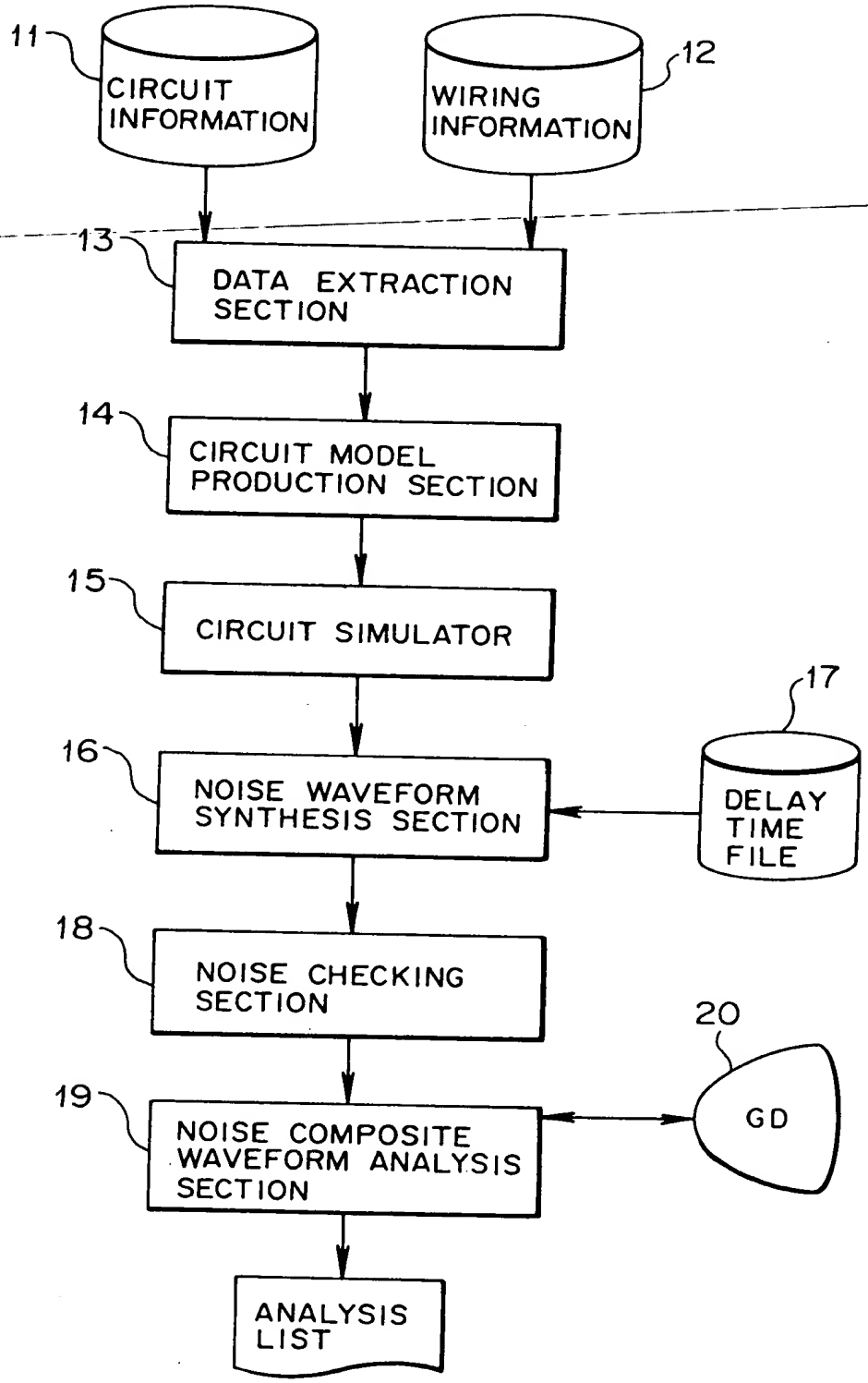
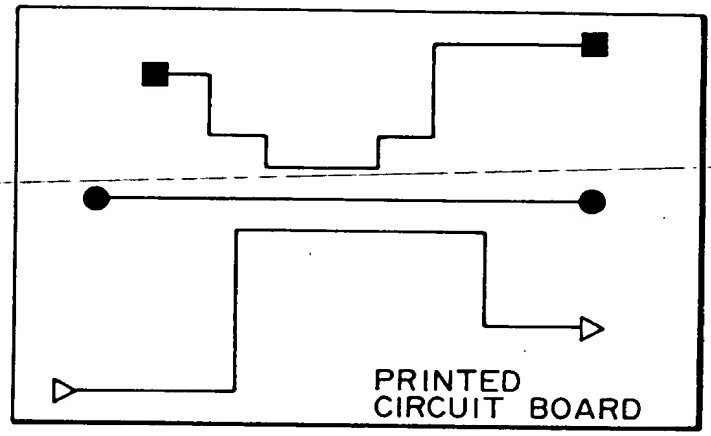


FIG.3A

Ded, Ding NET
CONFIGURATION EXAMPLE



Ded NET (Net A)
Ding NET (Net B)
Ding NET (Net C)

FIG.3B

ARRANGMENT OF
SIMULATION MODELS
(4 SIMULATIONS)

UP OF NetA (Ded)
DN OF NetA (Ded)
Net B (Ding)
Net C (Ding)

FIG.4

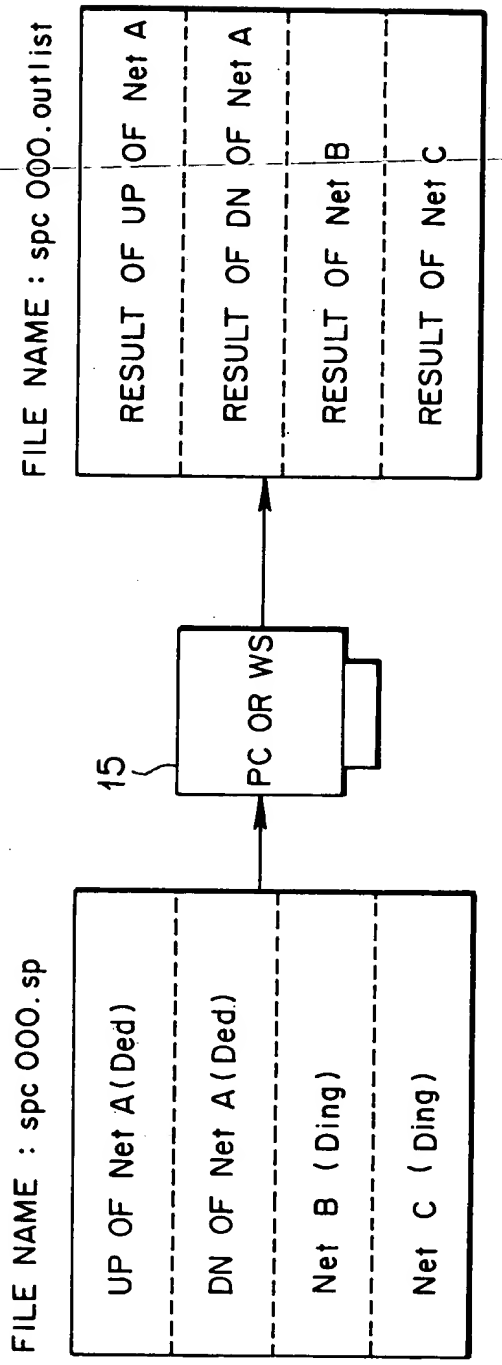
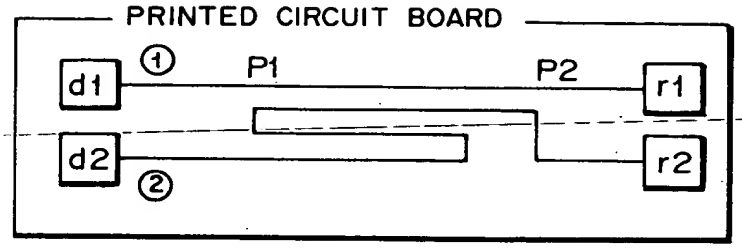

FILE NAME : spc 000.sp
UP OF Net A(Ded)
DN OF Net A(Ded)
Net B (Ding)
Net C (Ding)
15
PC OR WS
FILE NAME : spc 000.outlist
RESULT OF UP OF Net A
RESULT OF DN OF Net A
RESULT OF Net B
RESULT OF Net C

FIG. 5



① NOTICED NET (NET INFLUENCED BY NOISE)

② NOISE NET (NET HAVING INFLUENCE OF NOISE)

FIG. 6A

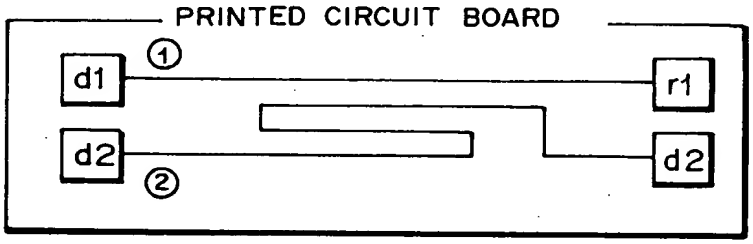


FIG. 6B

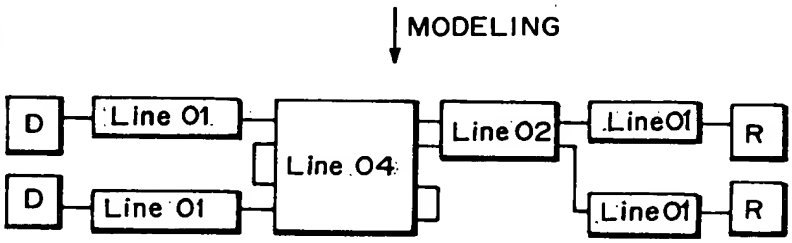
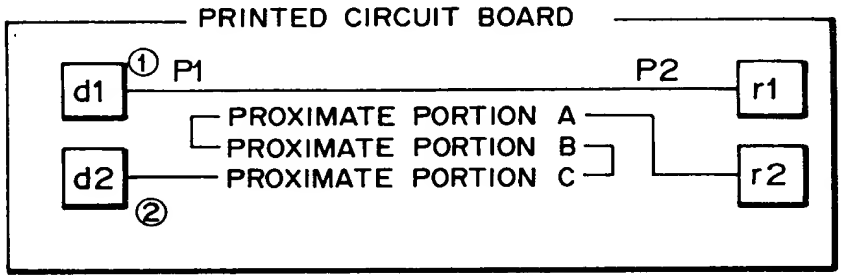


FIG. 7


PRINTED CIRCUIT BOARD
d1
①
P1
P2
r1
PROXIMATE PORTION A
PROXIMATE PORTION B
PROXIMATE PORTION C
d2
②
r2

FIRST, ONLY PROXIMATE PORTION A IS MODELED AS PARALLEL MODEL

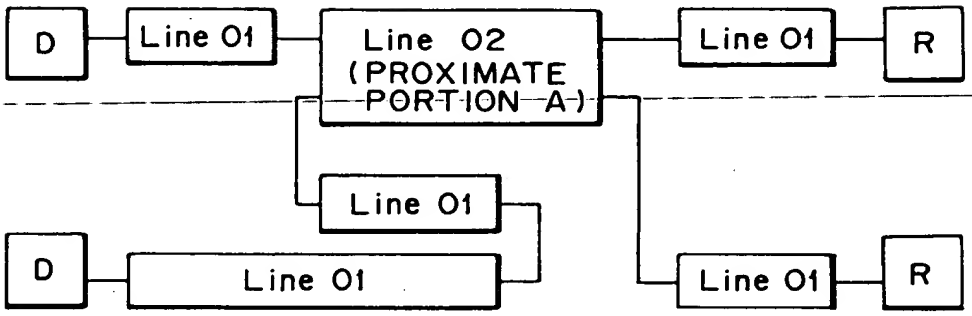


FIG.8A

NEXT, ONLY PROXIMATE PORTION B IS MODELED AS PARALLEL MODEL

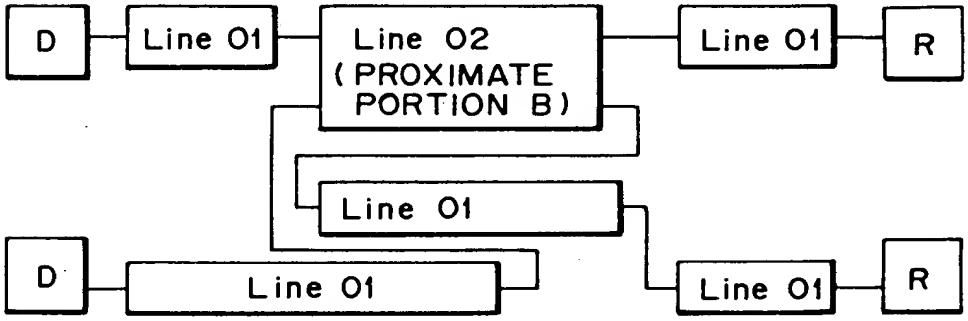


FIG.8B

FINALLY, ONLY PROXIMATE PORTION C IS MODELED AS PARALLEL MODEL

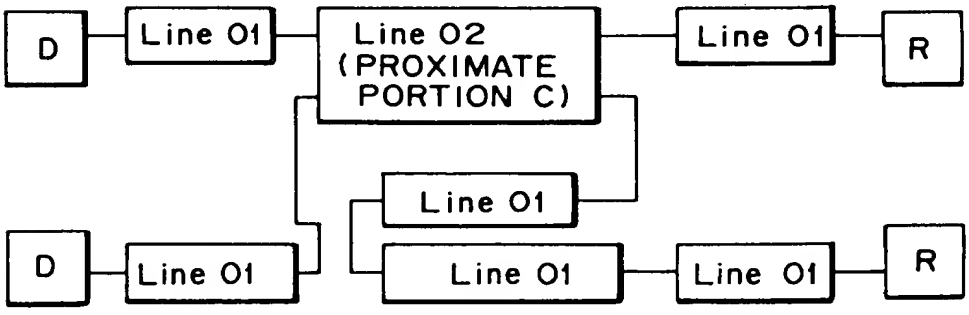


FIG.8C

FIG.9

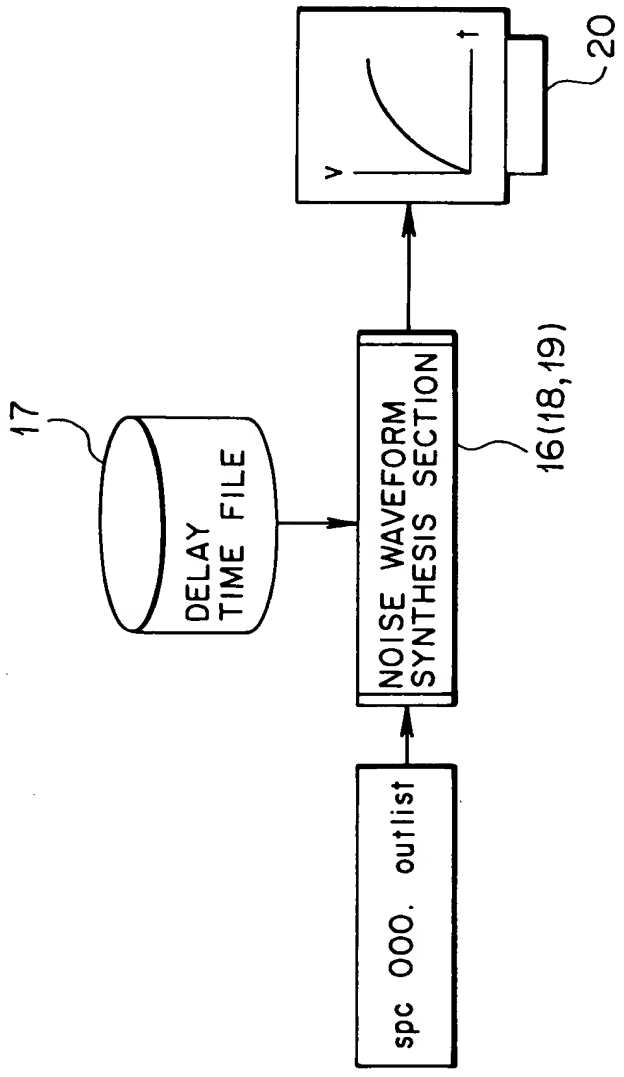

17
DELAY TIME FILE
NOISE WAVEFORM SYNTHESIS SECTION
16(18,19)
spc 000. outlist
v
t
20

FIG. 10A

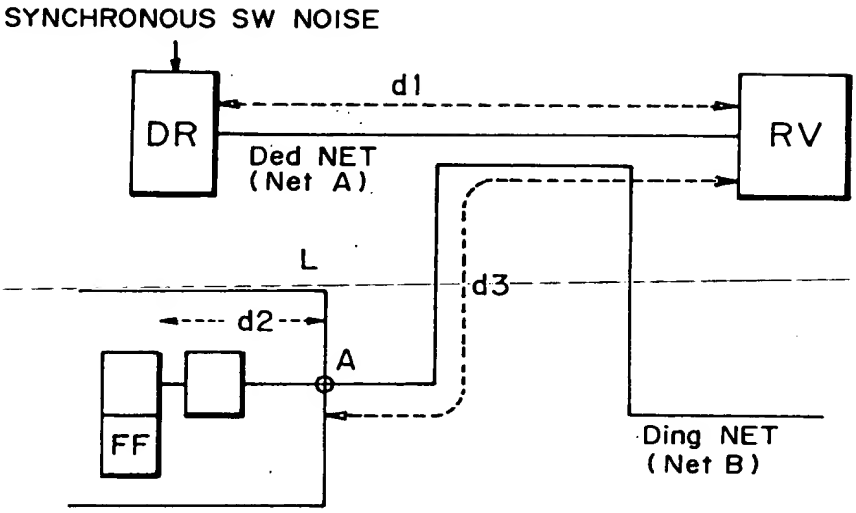


FIG. 10B

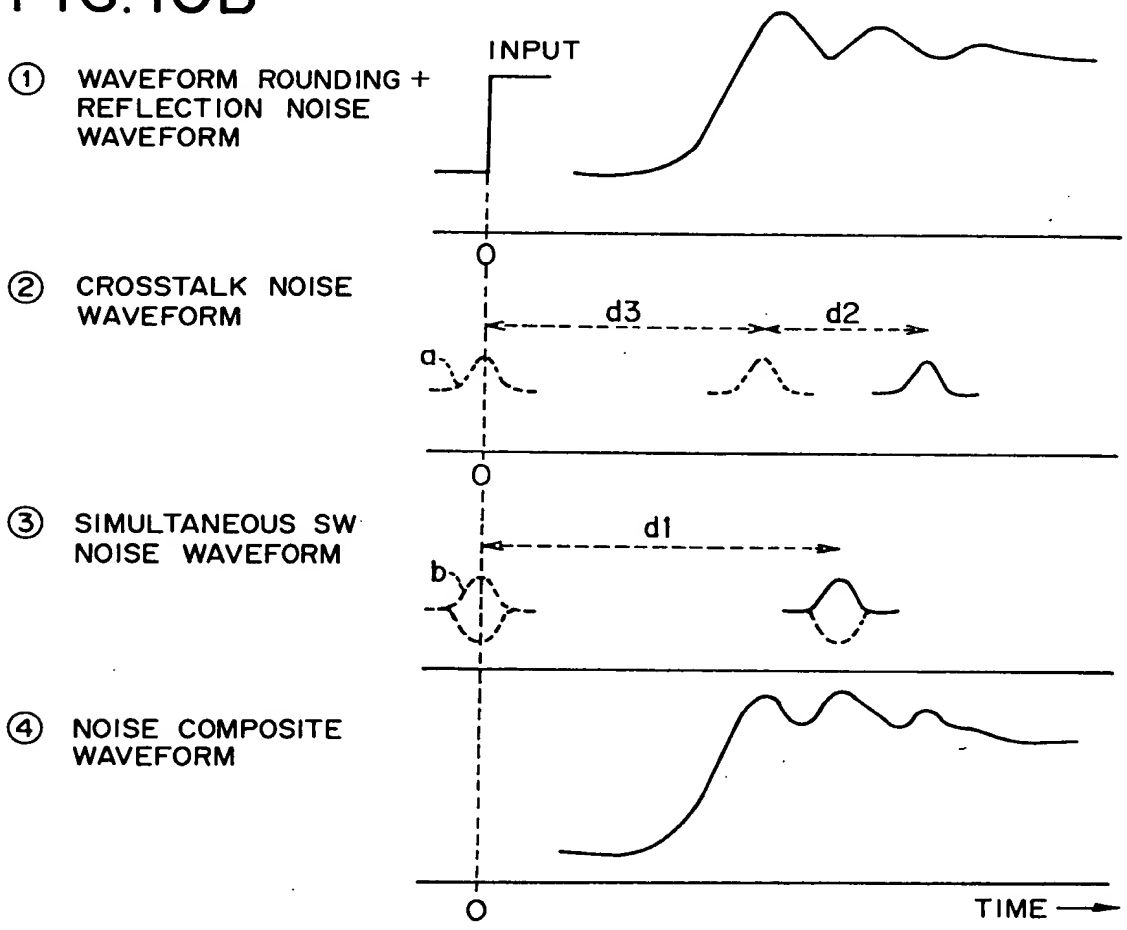


FIG. 11

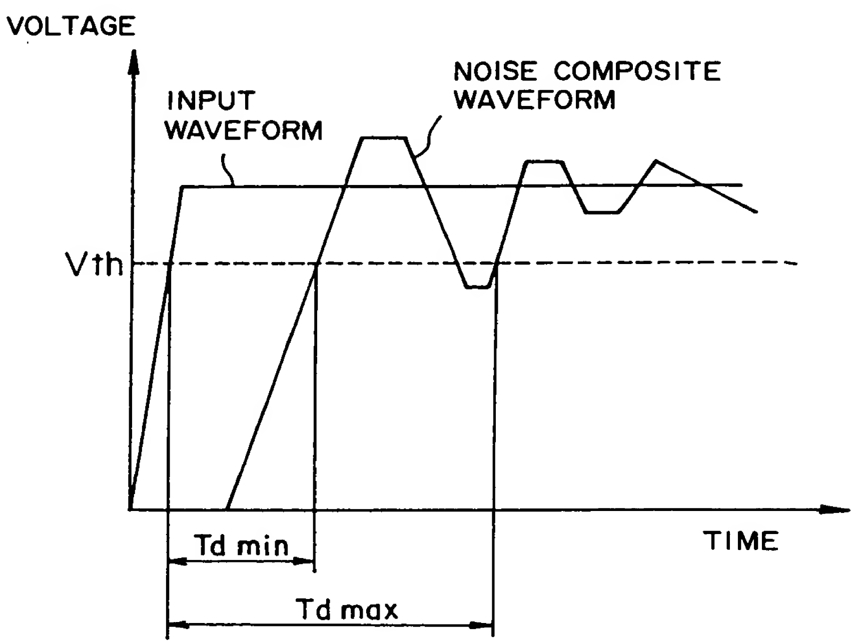

VOLTAGE
INPUT WAVEFORM
NOISE COMPOSITE WAVEFORM
Vth
TIME
Td min
Td max

FIG. 12

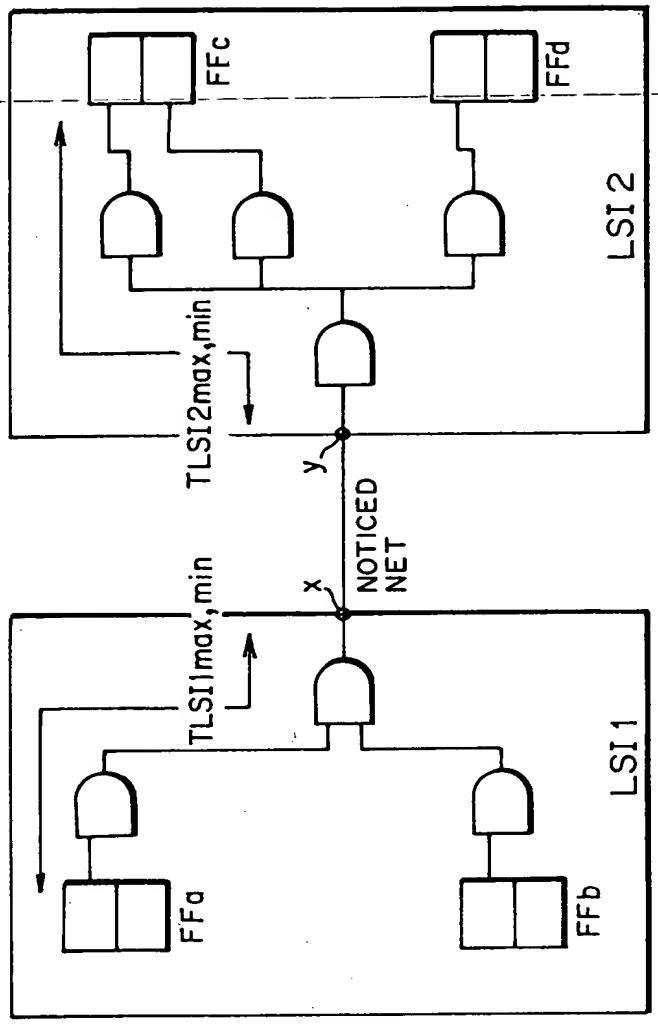

FFc
FFd
LSI 2
TLSI2max,min
y
NOTICED NET
x
TLSI1max,min
LSI 1
FFa
FFb

FIG. 13

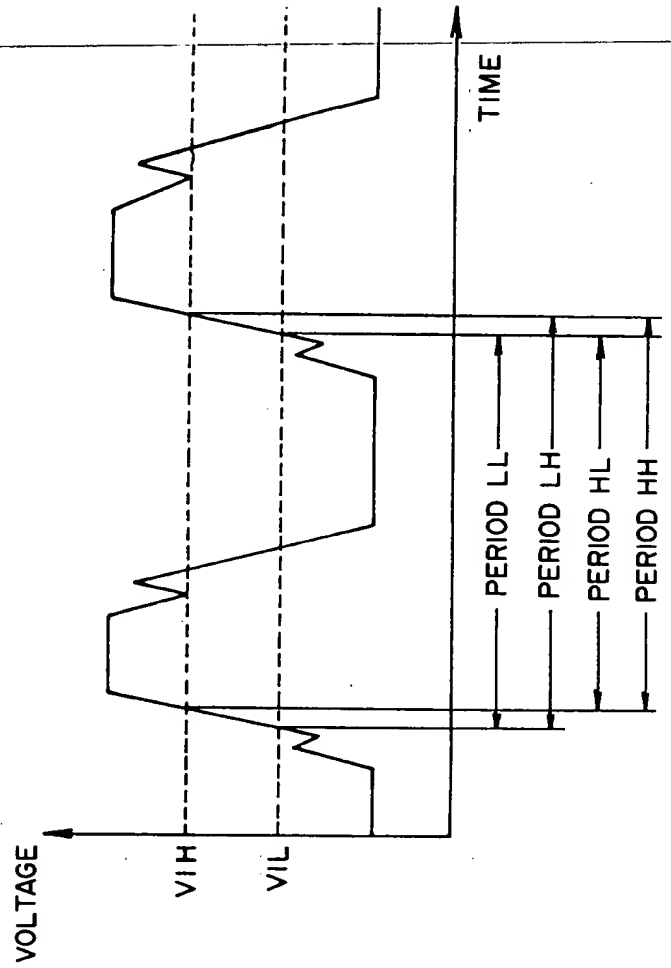


FIG. 14

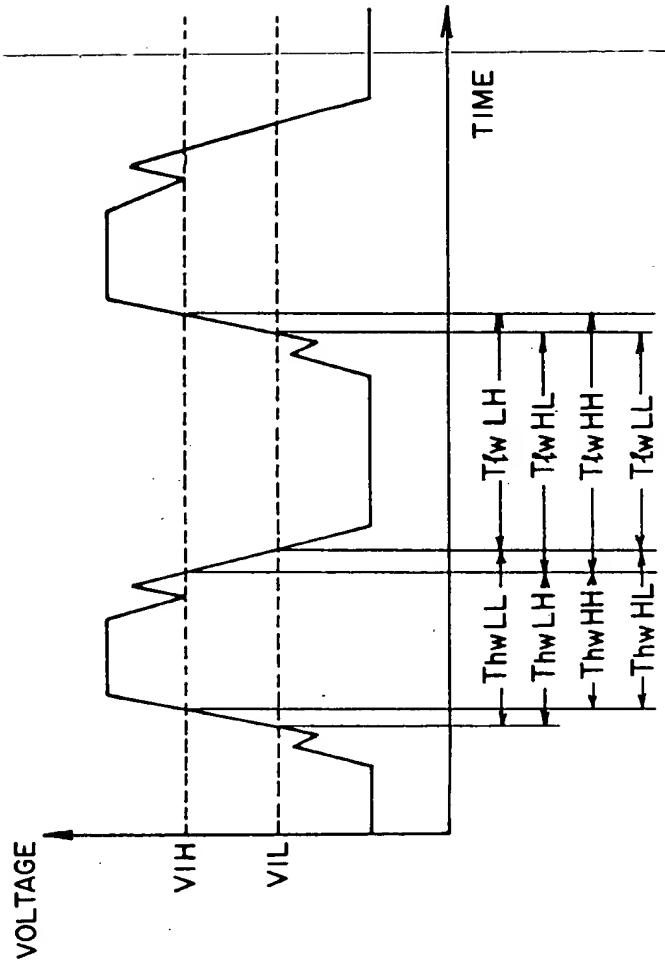

VOLTAGE
VIH
VIL
TIME
TfwLH
TfwHL
TfwHH
TfwLL
ThwLL
ThwLH
ThwHH
ThwHL

FIG. 15

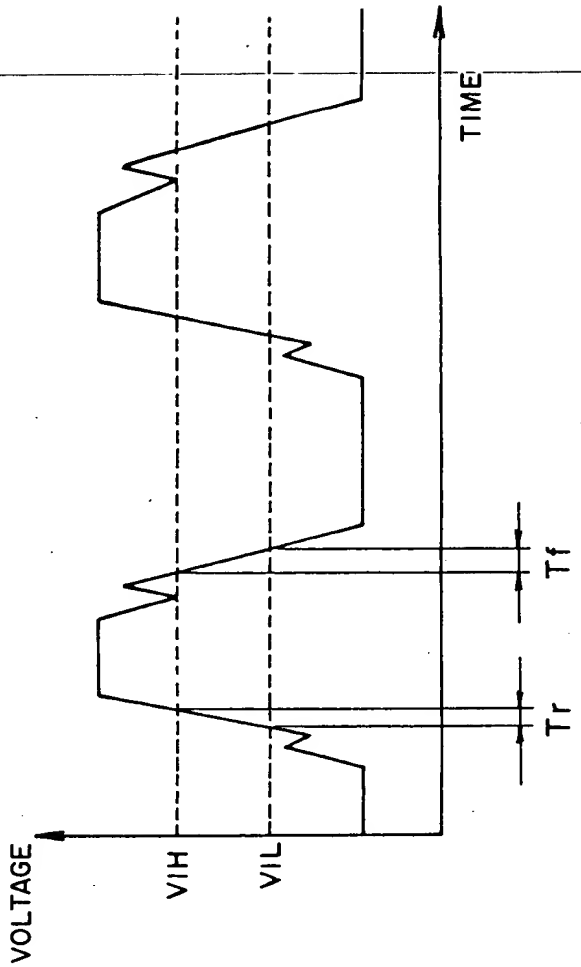


FIG. 16

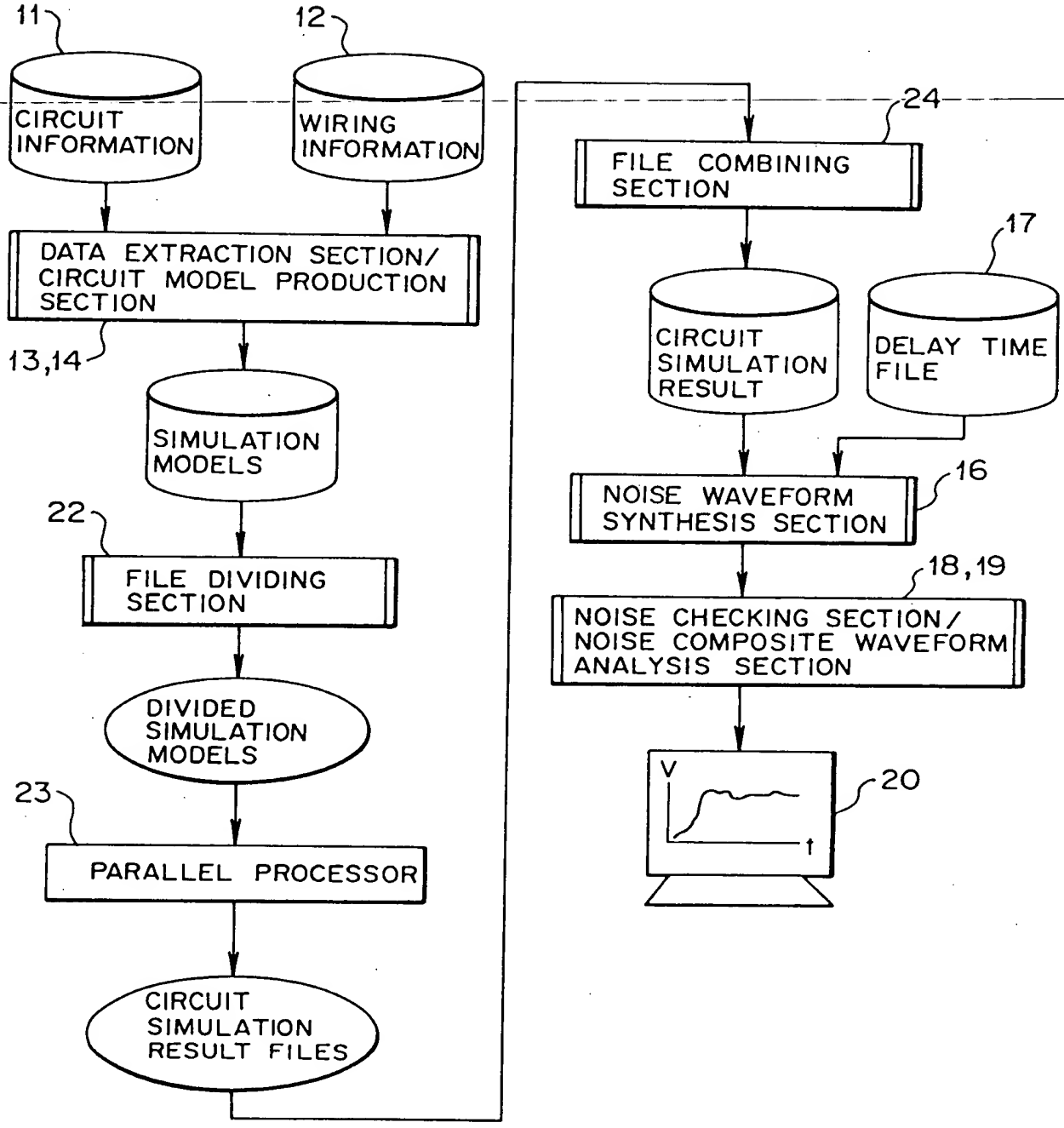

11
12
CIRCUIT INFORMATION
WIRING INFORMATION
DATA EXTRACTION SECTION/ CIRCUIT MODEL PRODUCTION SECTION
13,14
SIMULATION MODELS
22
FILE DIVIDING SECTION
DIVIDED SIMULATION MODELS
23
PARALLEL PROCESSOR
CIRCUIT SIMULATION RESULT FILES
24
FILE COMBINING SECTION
17
CIRCUIT SIMULATION RESULT
DELAY TIME FILE
NOISE WAVEFORM SYNTHESIS SECTION
16
18,19
NOISE CHECKING SECTION/ NOISE COMPOSITE WAVEFORM ANALYSIS SECTION
V
t
20

FIG. 17A

FILE NAME : spc 000.sp

UP OF Net A (Ded)
DN OF Net A (Ded)
Net B (Ding)
Net C (Ding)

FIG. 17B

FILE NAME : spc 000.sp.001

UP OF Net A (Ded)

FILE NAME : spc 000.sp.002

DN OF Net A (Ded)

FILE NAME : spc 000.sp.003

Net B (Ding)

FILE NAME : spc 000.sp.004

Net C (Ding)

FIG. 18

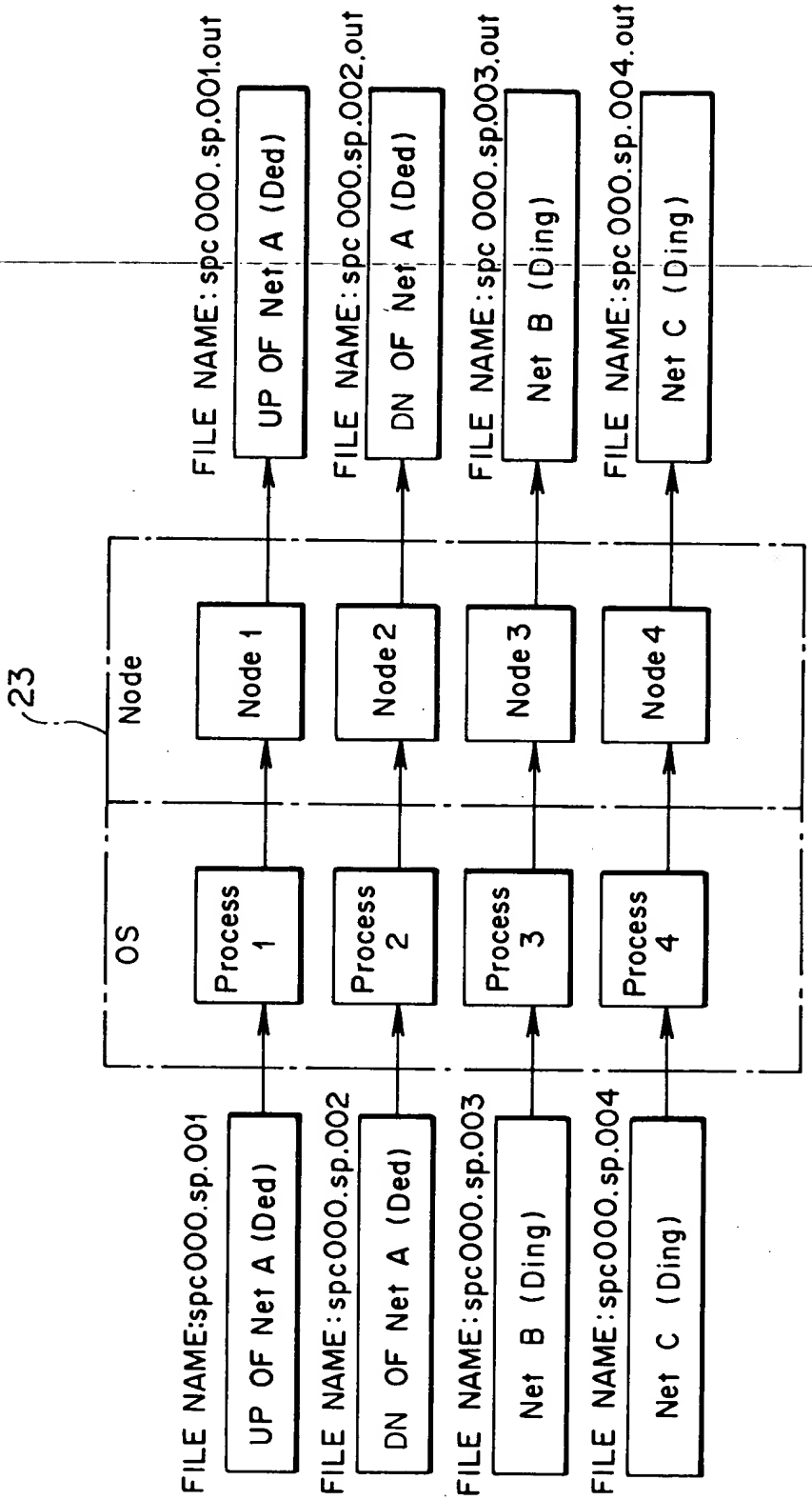

23
OS
Node
Process 1
Process 2
Process 3
Process 4
Node 1
Node 2
Node 3
Node 4
FILE NAME:spc000.sp.001
UP OF Net A (Ded)
FILE NAME:spc000.sp.002
DN OF Net A (Ded)
FILE NAME:spc000.sp.003
Net B (Ding)
FILE NAME:spc000.sp.004
Net C (Ding)
FILE NAME: spc 000.sp.001.out
UP OF Net A (Ded)
FILE NAME: spc 000.sp.002.out
DN OF Net A (Ded)
FILE NAME: spc 000.sp.003.out
Net B (Ding)
FILE NAME: spc 000.sp.004.out
Net C (Ding)

FIG. 19

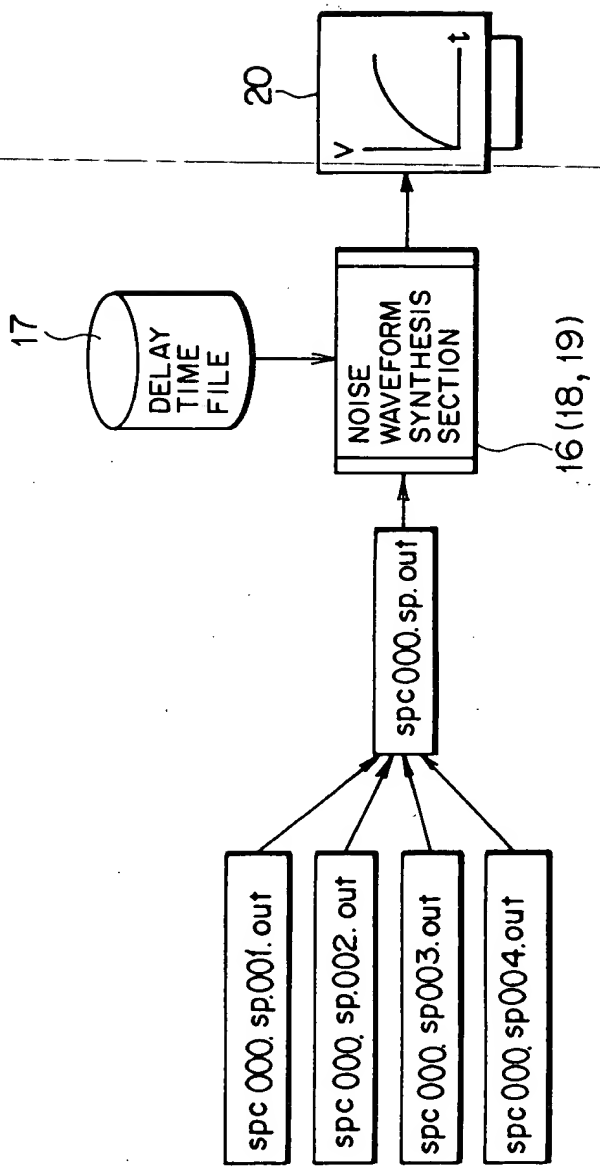

20
v
t
17
DELAY TIME FILE
NOISE WAVEFORM SYNTHESIS SECTION
16 (18, 19)
spc000.sp.out
spc 000. sp.001. out
spc 000. sp.002. out
spc 000. sp003. out
spc 000. sp004. out

FIG. 20

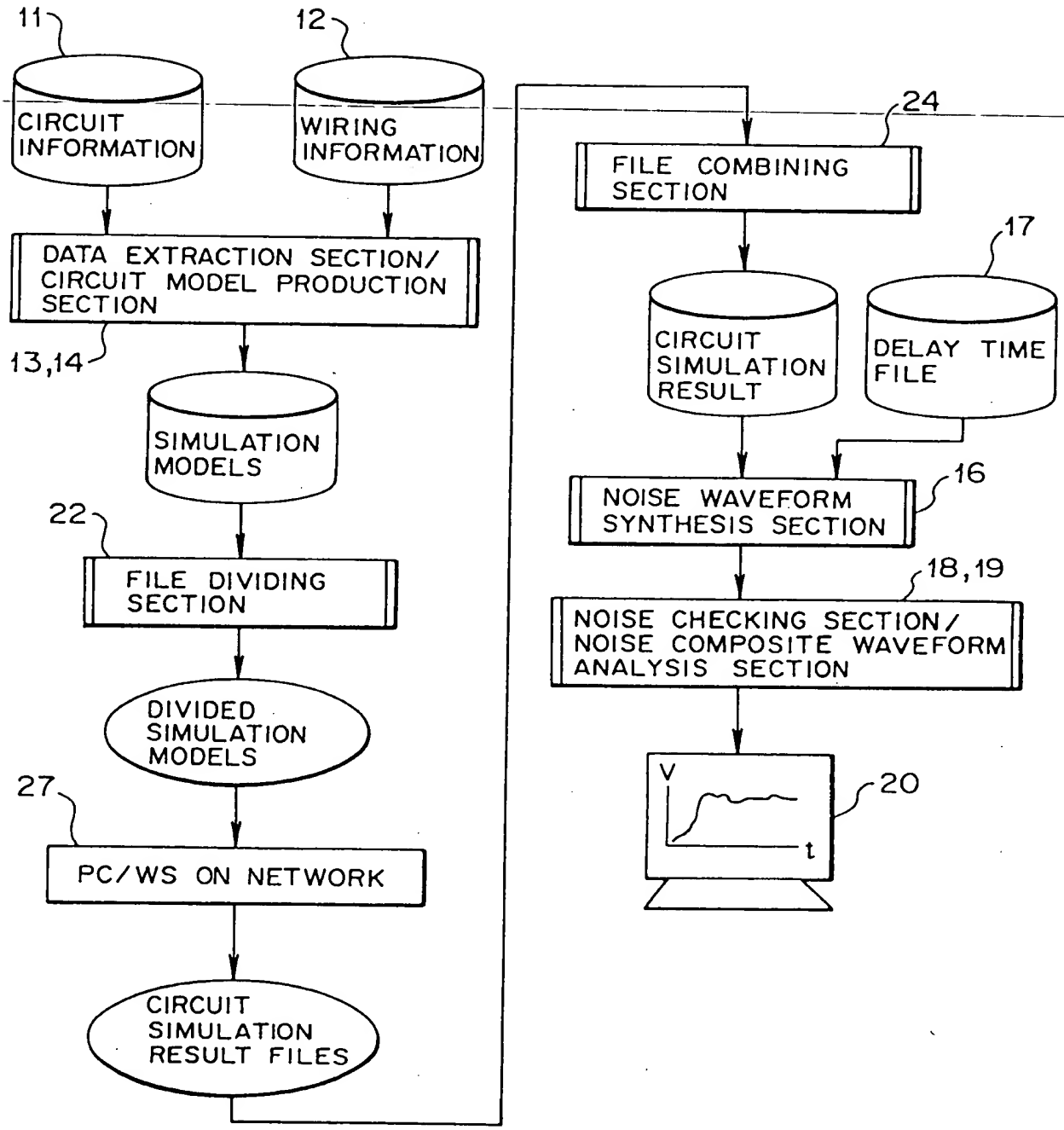

11
12
CIRCUIT INFORMATION
WIRING INFORMATION
DATA EXTRACTION SECTION/ CIRCUIT MODEL PRODUCTION SECTION
13,14
SIMULATION MODELS
22
FILE DIVIDING SECTION
DIVIDED SIMULATION MODELS
27
PC/WS ON NETWORK
CIRCUIT SIMULATION RESULT FILES
24
FILE COMBINING SECTION
17
CIRCUIT SIMULATION RESULT
DELAY TIME FILE
NOISE WAVEFORM SYNTHESIS SECTION
16
18,19
NOISE CHECKING SECTION/ NOISE COMPOSITE WAVEFORM ANALYSIS SECTION
V
t
20

FIG.21A

FILE NAME : spc 000. sp

UP OF Net A (Ded)
DN OF Net A (Ded)
Net B (Ding)
Net C (Ding)

FIG.21B

FILE NAME : spc 000. sp.001

UP OF Net A (Ded)
DN OF Net A (Ded)

FILE NAME : spc 000. sp.002

Net B (Ding)
Net C (Ding)

FIG. 22

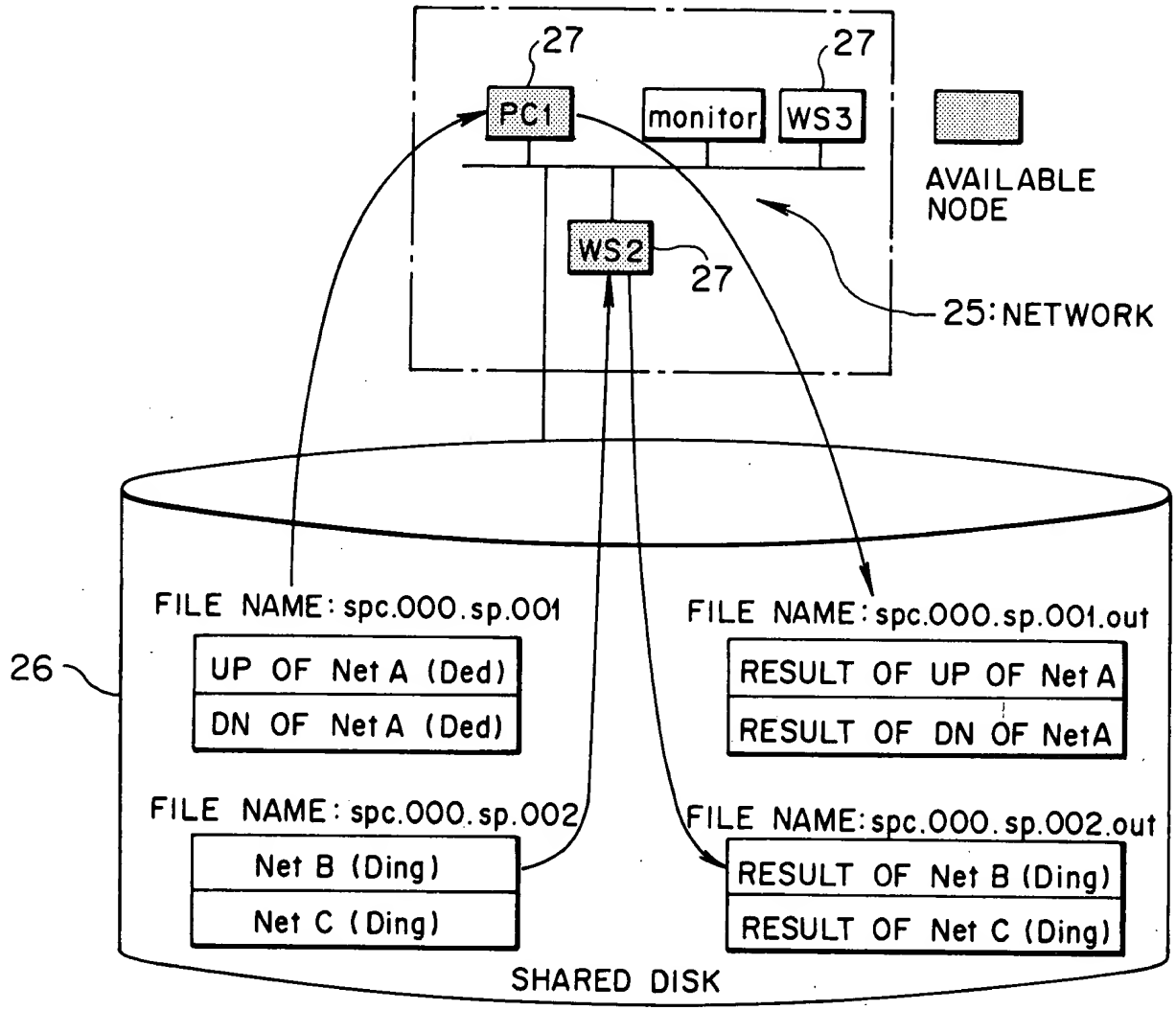

27
27
PC1
monitor
WS3
AVAILABLE NODE
WS2
27
25: NETWORK
26
FILE NAME: spc.000.sp.001
UP OF Net A (Ded)
DN OF Net A (Ded)
FILE NAME: spc.000.sp.001.out
RESULT OF UP OF Net A
RESULT OF DN OF NetA
FILE NAME: spc.000.sp.002
Net B (Ding)
Net C (Ding)
FILE NAME: spc.000.sp.002.out
RESULT OF Net B (Ding)
RESULT OF Net C (Ding)
SHARED DISK

FIG.23

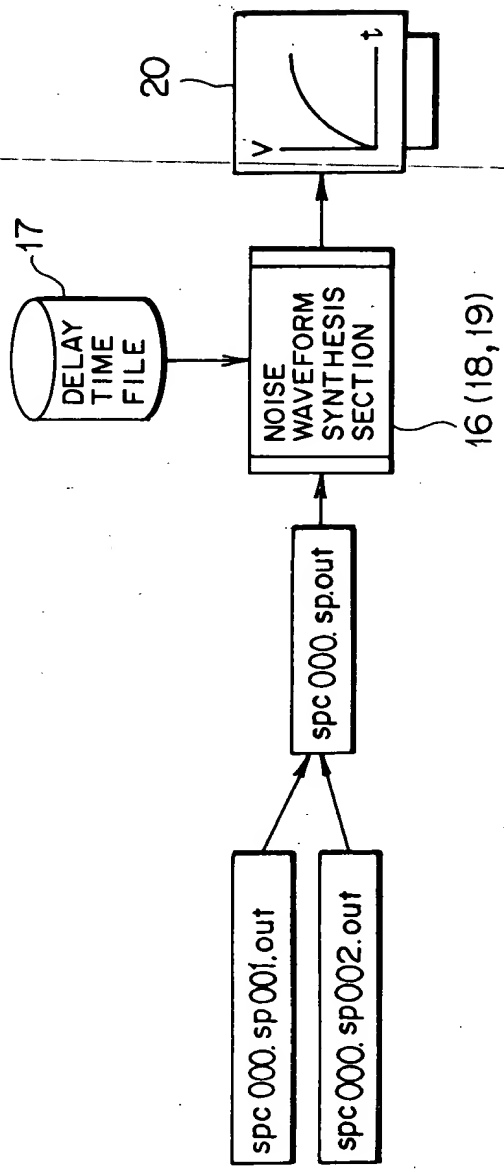

20
v
t
17
DELAY TIME FILE
NOISE WAVEFORM SYNTHESIS SECTION
16 (18, 19)
spc 000. sp.out
spc 000. sp001. out
spc 000. sp002. out

FIG. 24

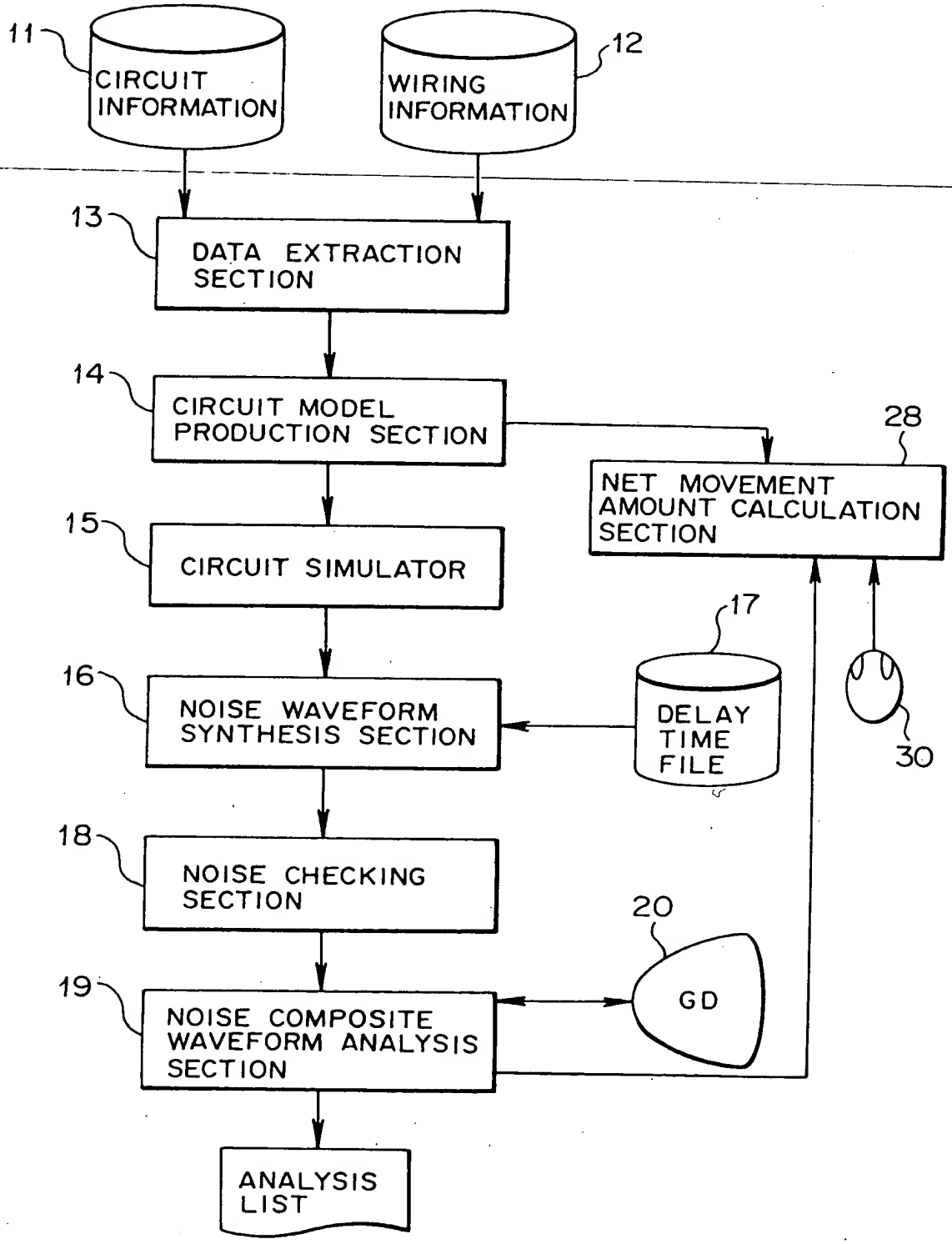

11
CIRCUIT INFORMATION
12
WIRING INFORMATION
13
DATA EXTRACTION SECTION
14
CIRCUIT MODEL PRODUCTION SECTION
28
NET MOVEMENT AMOUNT CALCULATION SECTION
15
CIRCUIT SIMULATOR
17
16
NOISE WAVEFORM SYNTHESIS SECTION
DELAY TIME FILE
30
18
NOISE CHECKING SECTION
20
GD
19
NOISE COMPOSITE WAVEFORM ANALYSIS SECTION
ANALYSIS LIST

FIG. 25A

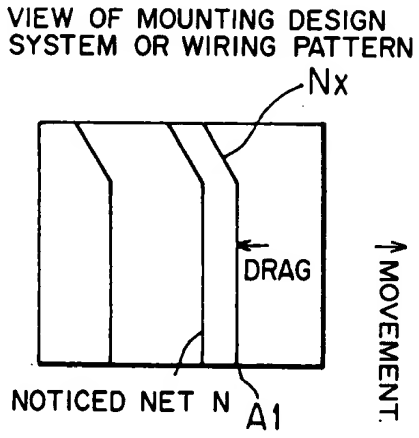


FIG. 25B

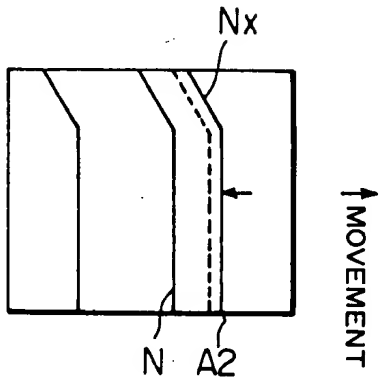


FIG. 25C

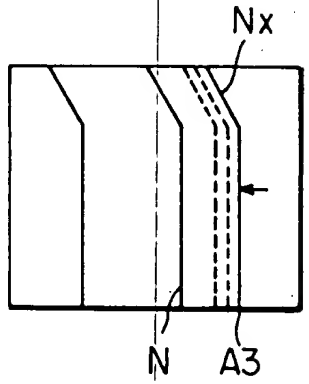


FIG. 25D

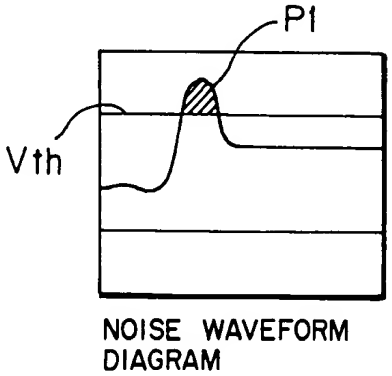


FIG. 25E

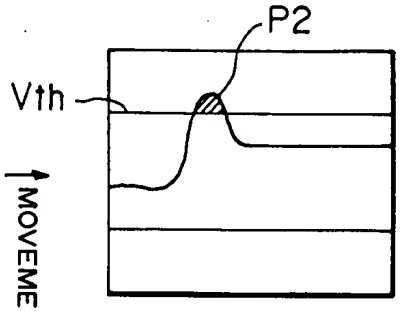


FIG. 25F

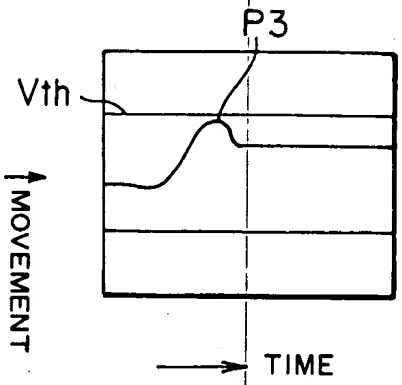


FIG. 26

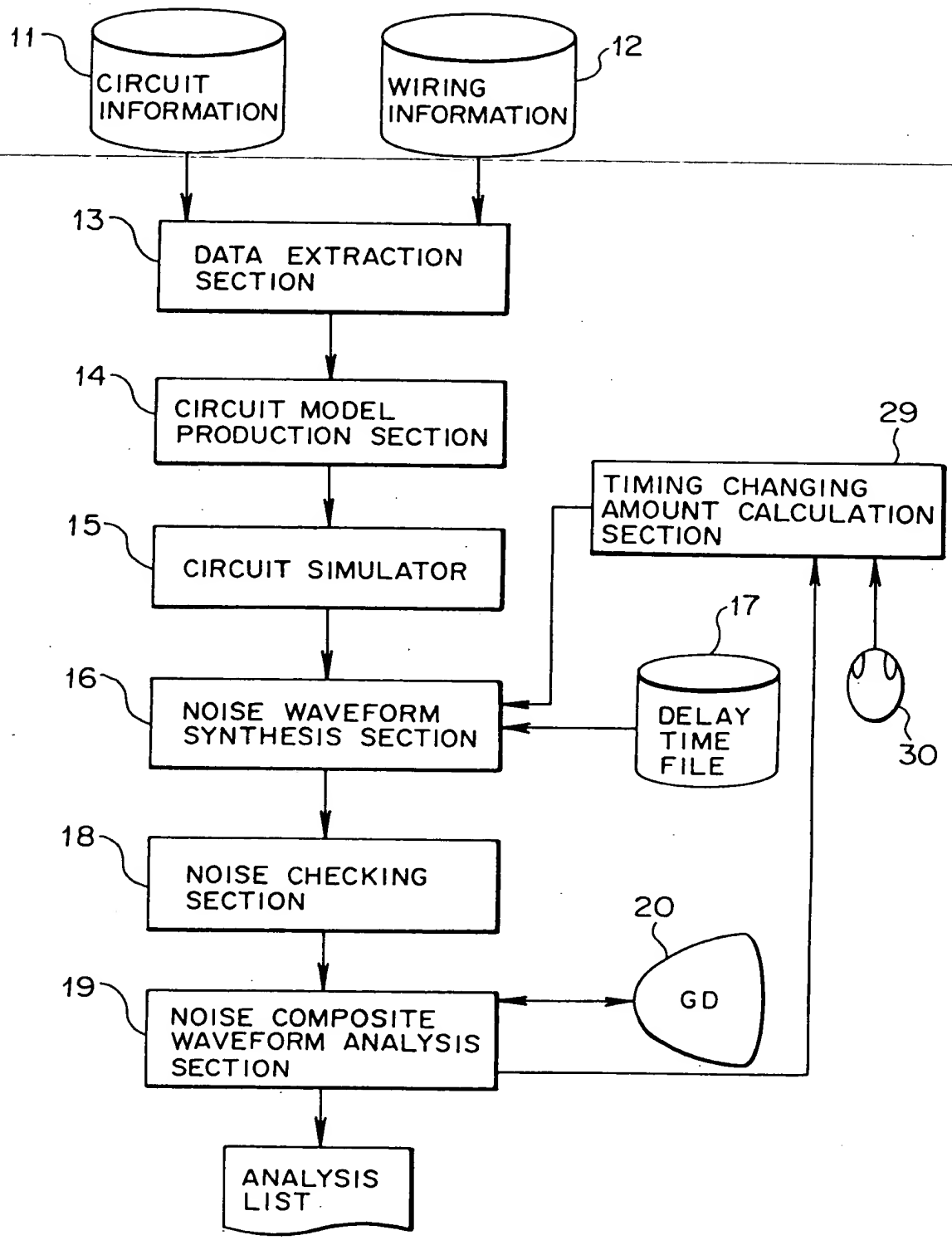

11
CIRCUIT INFORMATION
12
WIRING INFORMATION
13
DATA EXTRACTION SECTION
14
CIRCUIT MODEL PRODUCTION SECTION
15
CIRCUIT SIMULATOR
16
NOISE WAVEFORM SYNTHESIS SECTION
17
DELAY TIME FILE
18
NOISE CHECKING SECTION
19
NOISE COMPOSITE WAVEFORM ANALYSIS SECTION
20
GD
29
TIMING CHANGING AMOUNT CALCULATION SECTION
30
ANALYSIS LIST

FIG. 27

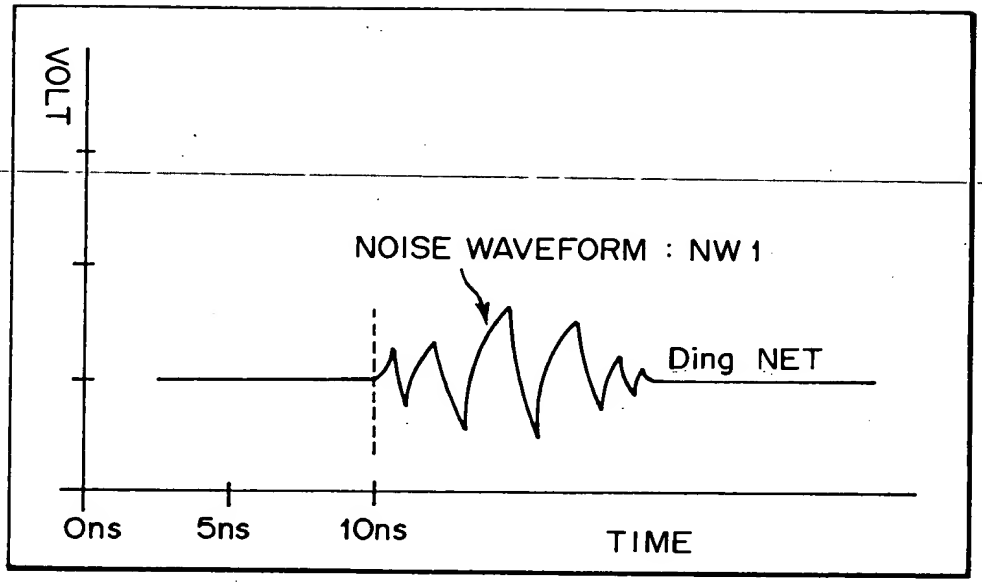

VOLT
NOISE WAVEFORM : NW1
Ding NET
0ns
5ns
10ns
TIME

FIG. 28

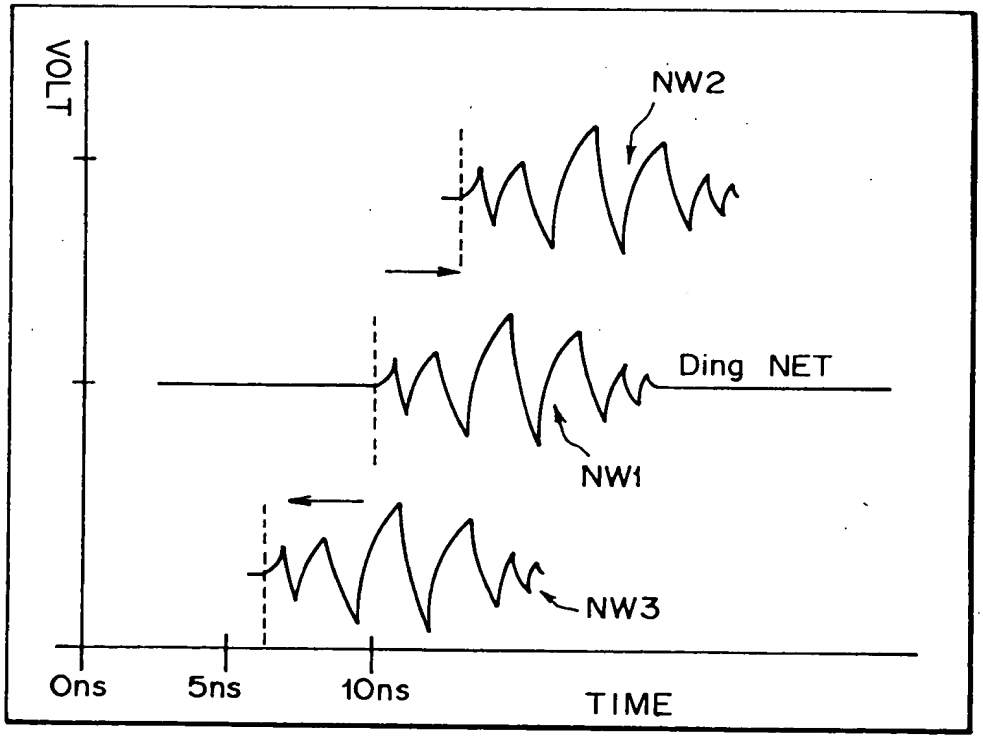

VOLT
NW2
Ding NET
NW1
NW3
0ns
5ns
10ns
TIME

FIG. 29

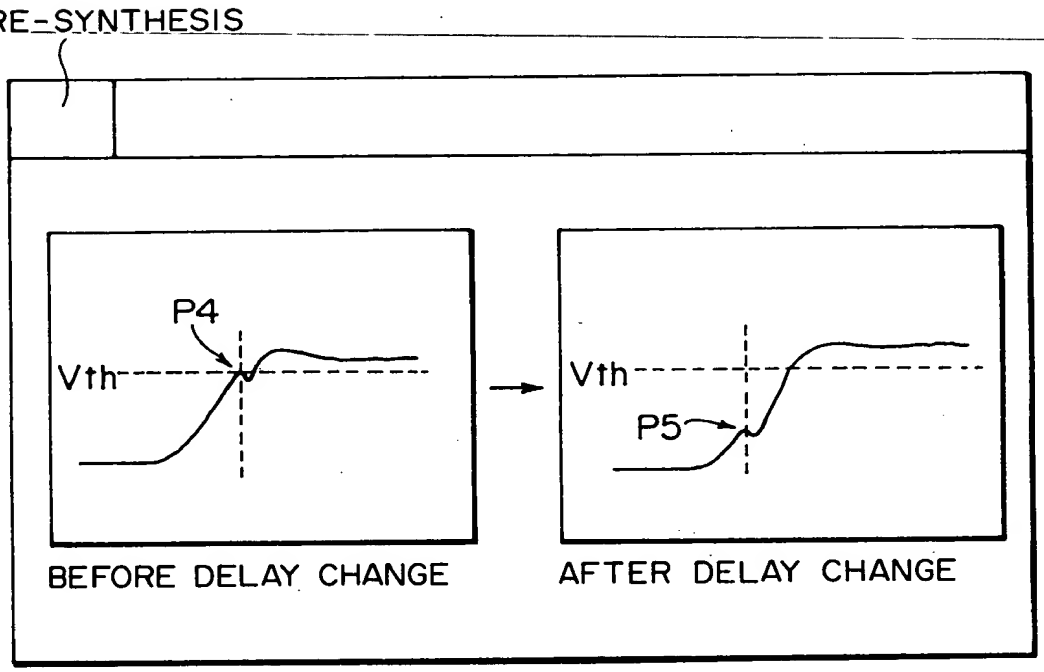

RE-SYNTHESIS
P4
Vth
P5
Vth
BEFORE DELAY CHANGE
AFTER DELAY CHANGE

FIG. 30

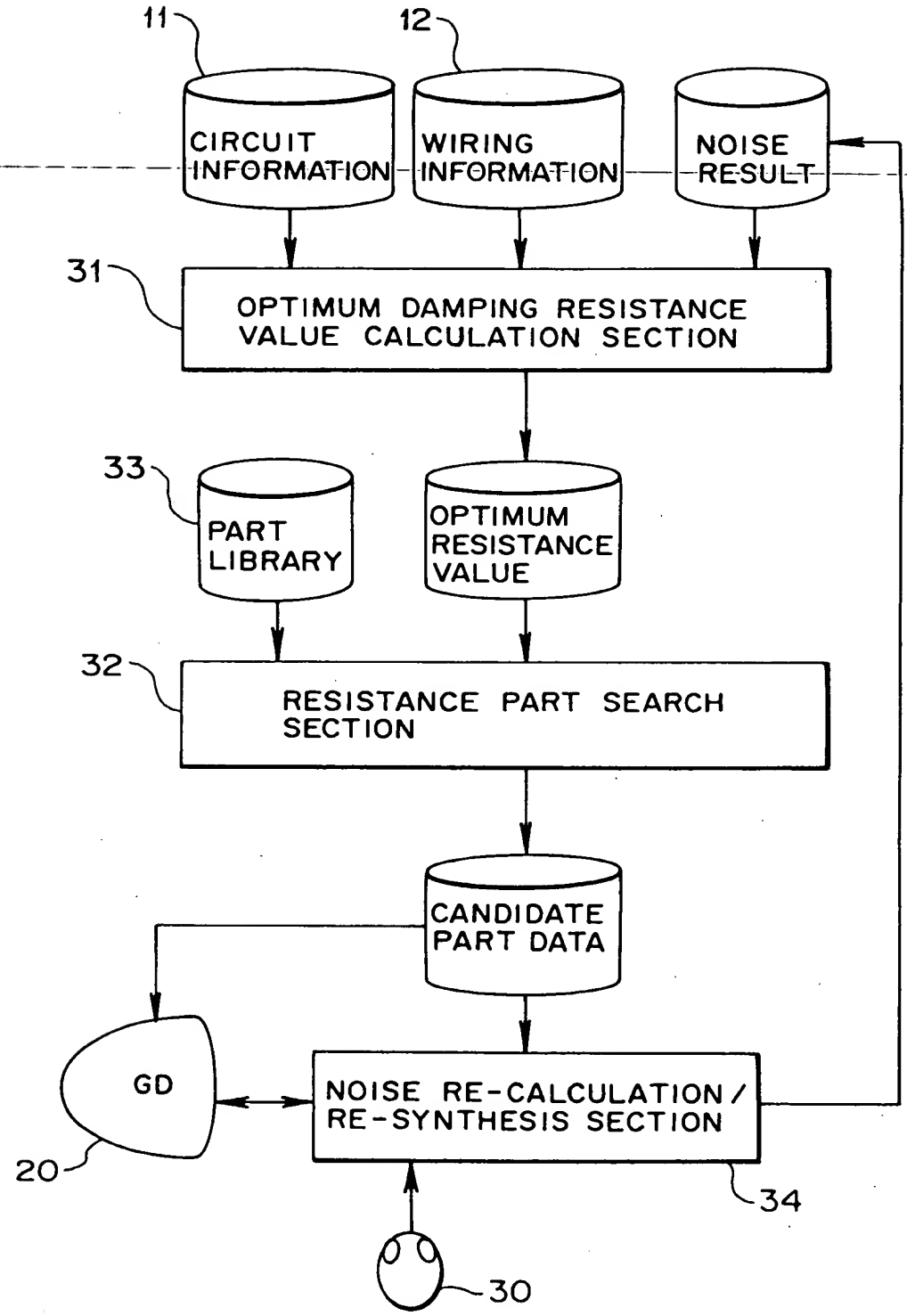

11
12
CIRCUIT INFORMATION
WIRING INFORMATION
NOISE RESULT
31
OPTIMUM DAMPING RESISTANCE VALUE CALCULATION SECTION
33
PART LIBRARY
OPTIMUM RESISTANCE VALUE
32
RESISTANCE PART SEARCH SECTION
CANDIDATE PART DATA
GD
20
NOISE RE-CALCULATION / RE-SYNTHESIS SECTION
34
30

FIG. 31

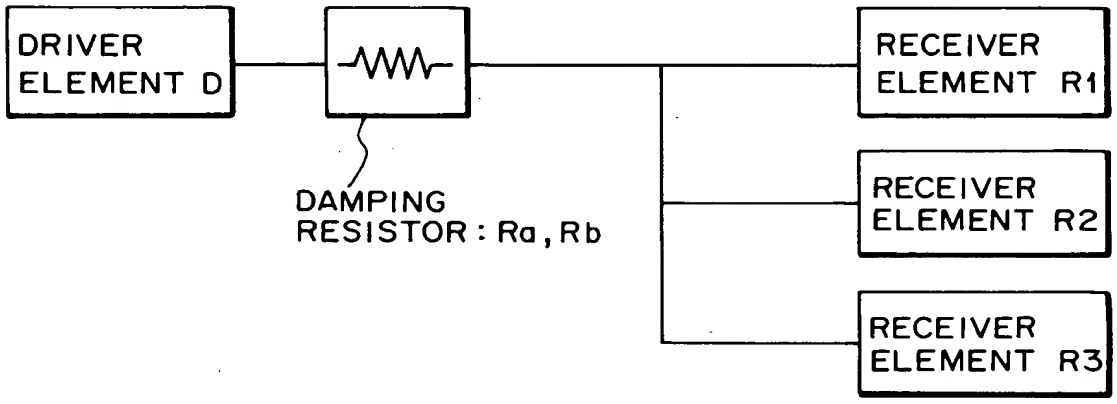

DRIVER
ELEMENT D
DAMPING
RESISTOR : Ra, Rb
RECEIVER
ELEMENT R1
RECEIVER
ELEMENT R2
RECEIVER
ELEMENT R3

FIG. 32

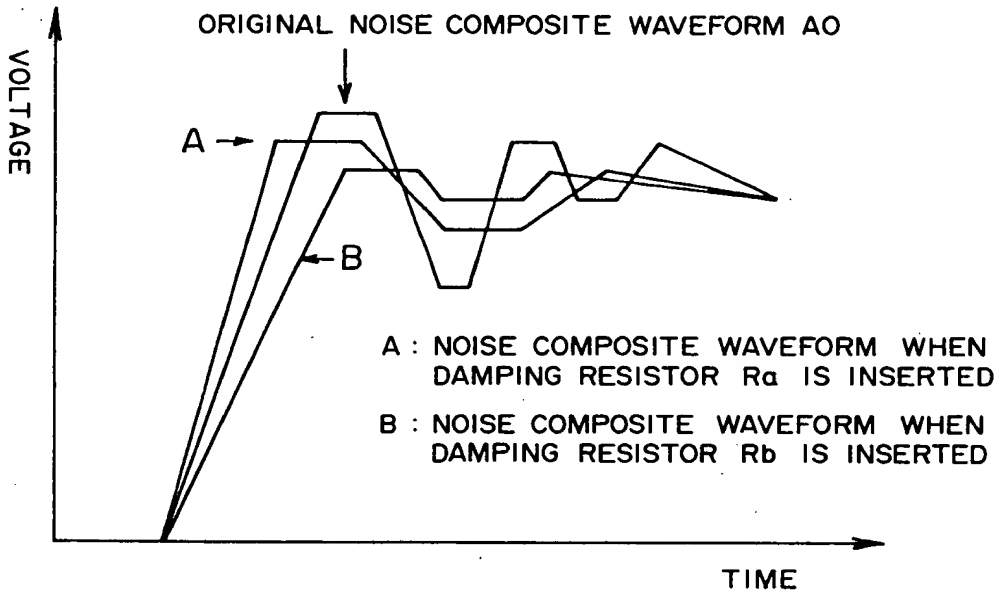

ORIGINAL NOISE COMPOSITE WAVEFORM AO
VOLTAGE
A
B
A : NOISE COMPOSITE WAVEFORM WHEN DAMPING RESISTOR Ra IS INSERTED
B : NOISE COMPOSITE WAVEFORM WHEN DAMPING RESISTOR Rb IS INSERTED
TIME

FIG. 33A

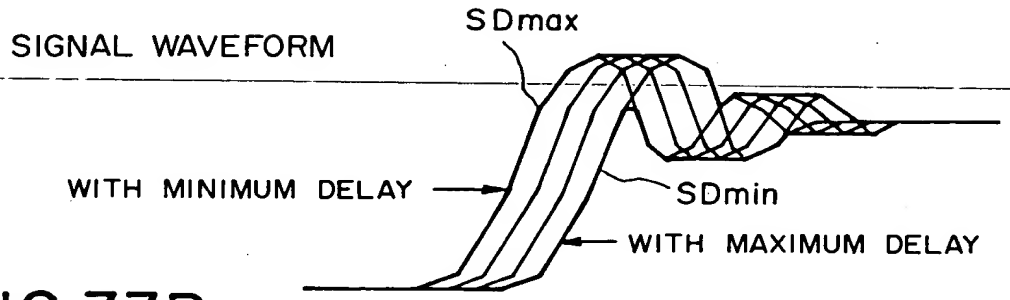


FIG. 33B

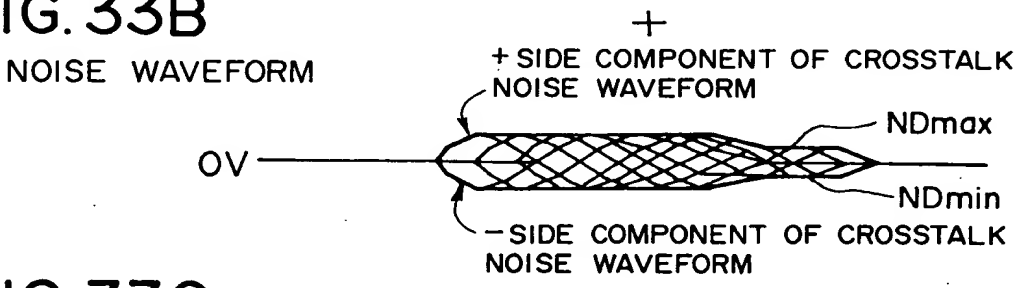


FIG. 33C

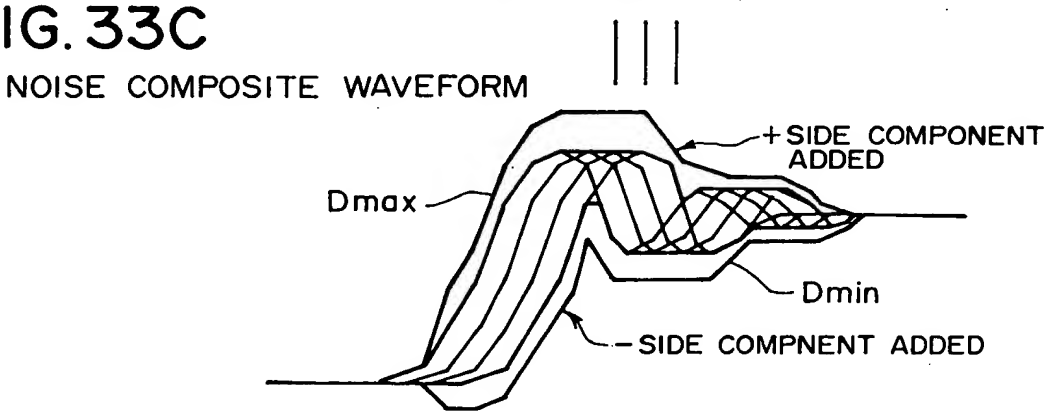


FIG. 34

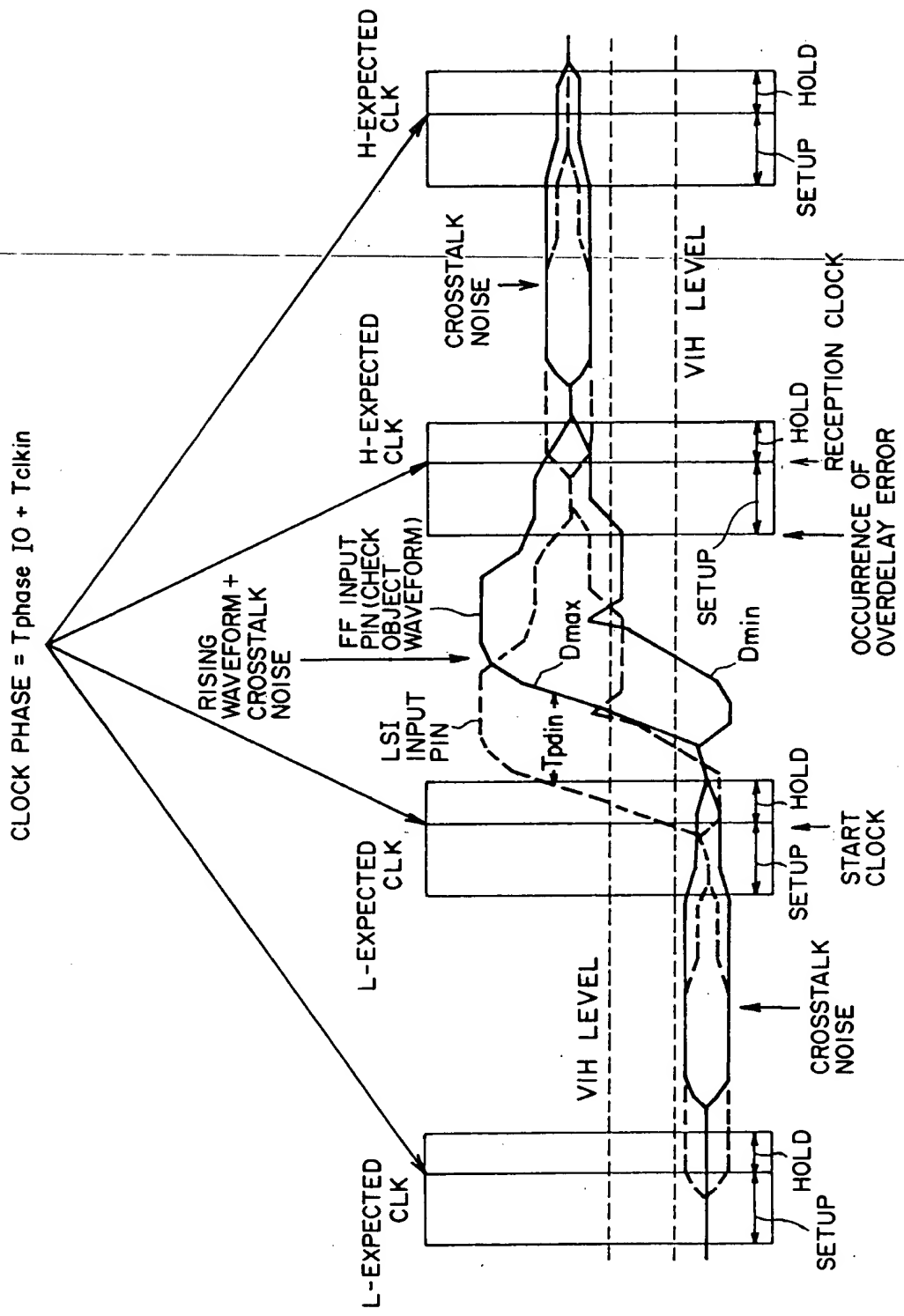

CLOCK PHASE = Tphase IO + Tclkin
H-EXPECTED CLK
H-EXPECTED CLK
L-EXPECTED CLK
L-EXPECTED CLK
CROSSTALK NOISE
VIH LEVEL
SETUP
HOLD
RISING WAVEFORM + CROSSTALK NOISE
FF INPUT PIN (CHECK OBJECT WAVEFORM)
LSI INPUT PIN
Tpdin
Dmax
Dmin
SETUP
HOLD
RECEPTION CLOCK
OCCURRENCE OF OVERDELAY ERROR
START CLOCK
CROSSTALK NOISE
VIH LEVEL
SETUP
HOLD

FIG. 35

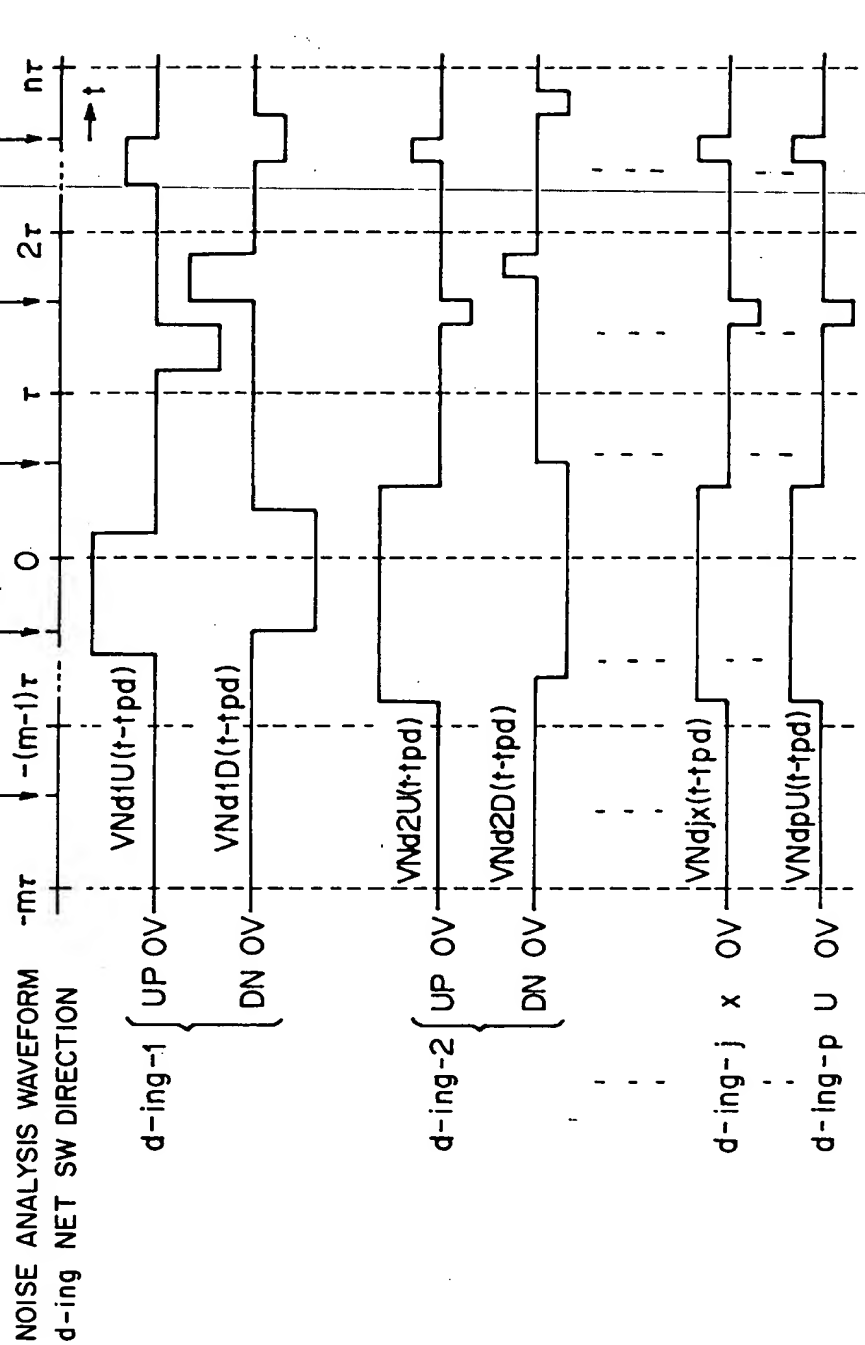

NOISE ANALYSIS WAVEFORM
d-ing NET SW DIRECTION
-mτ
tphase-mτ
-(m-1)τ
tphase-τ
0
tphase
τ
tphase+τ
2τ
tphase+(n-1)τ
nτ
t
VNd1U(t-tpd)
VNd1D(t-tpd)
VNd2U(t-tpd)
VNd2D(t-tpd)
VNdjx(t-tpd)
VNdpU(t-tpd)
d-ing-1
UP OV
DN OV
d-ing-2
UP OV
DN OV
d-ing-j x OV
d-ing-p U OV

FIG. 36

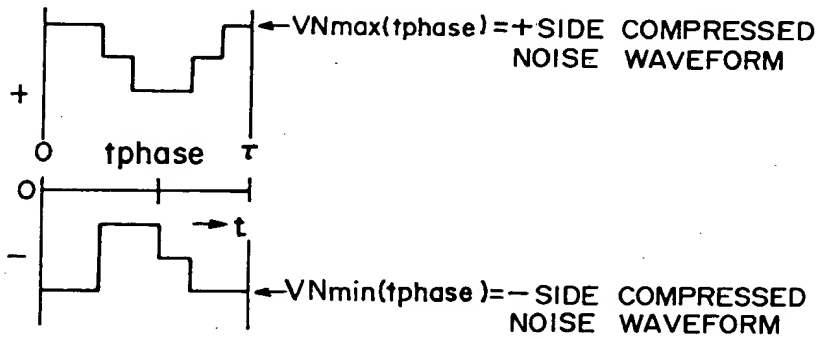

VNmax(tphase)=+SIDE COMPRESSED NOISE WAVEFORM
+
0
tphase
τ
0
t
−
VNmin(tphase)=− SIDE COMPRESSED NOISE WAVEFORM

FIG.37A LSI DR SIMULTANEOUS SW NOISE

FIG.37B LSI RV SIMULTANEOUS SW NOISE

FIG.37C PARALLEL WIRING PATTERN CROSSTALK NOISE
+CROSSING WIRING CROSSTALK NOISE

FIG.37D
- VIA CROSSTALK NOISE
- TERMINATING RESISTOR SIMULTANEOUS SW NOISE
- CONNECTOR CROSSTALK NOISE
- CABLE CROSSTALK NOISE
- DC NOISE

FIG.37E COMPOSITE NOISE WAVEFORM

FIG.37F TRANSMISSION WAVEFORM OF NOTICED NET
(UPON RISING)

FIG.37G COMPOSITE TRANSMISSION WAVEFORM OF NOISES
OF NOTICED NET (NOISE COMPOSITE WAVEFORM)

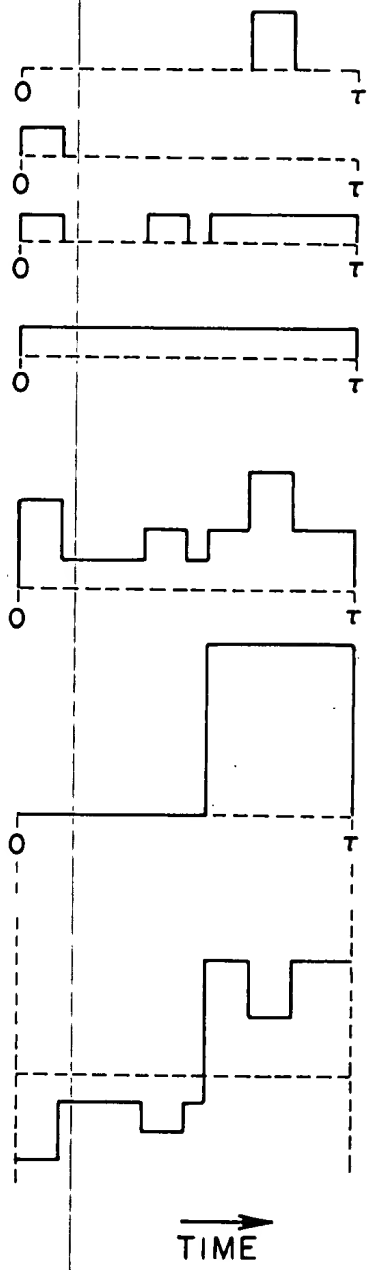


FIG. 38

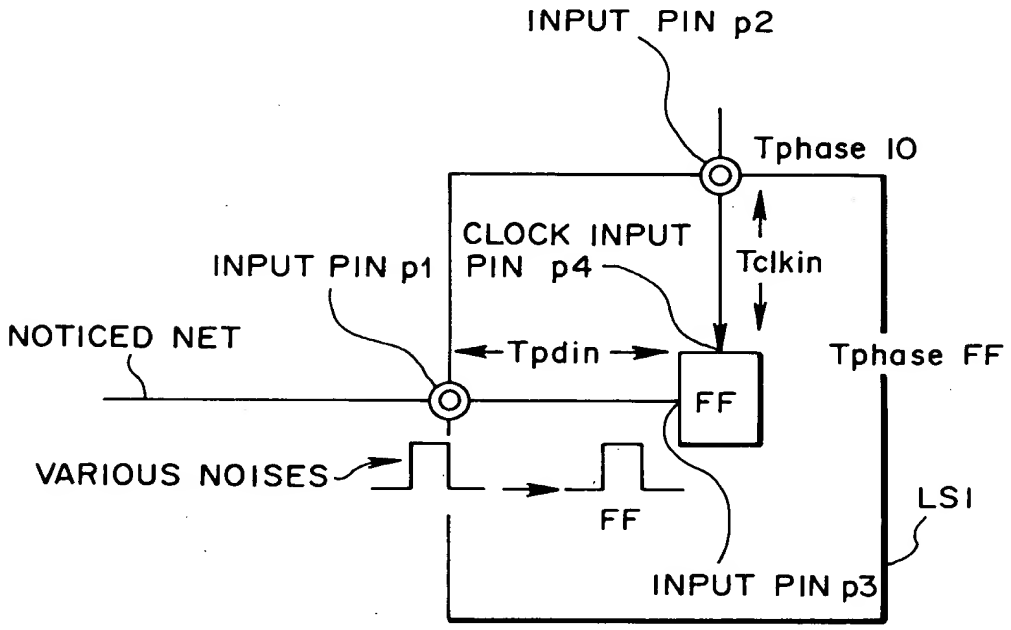

INPUT PIN p2
Tphase 10
CLOCK INPUT
PIN p4
Tclkin
INPUT PIN p1
NOTICED NET
Tpdin
Tphase FF
FF
VARIOUS NOISES
FF
LSI
INPUT PIN p3

FIG. 39A

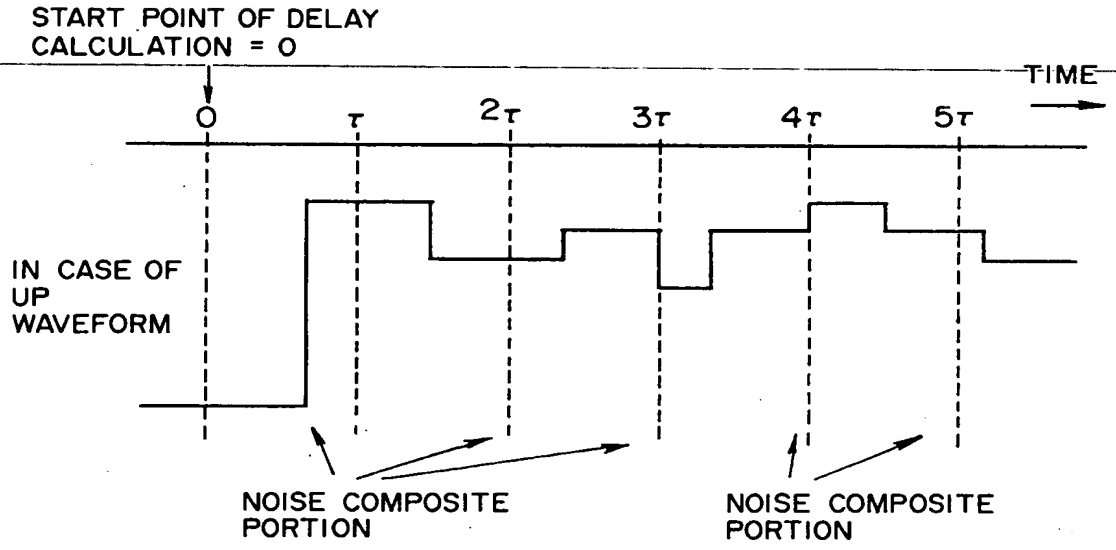


FIG. 39B

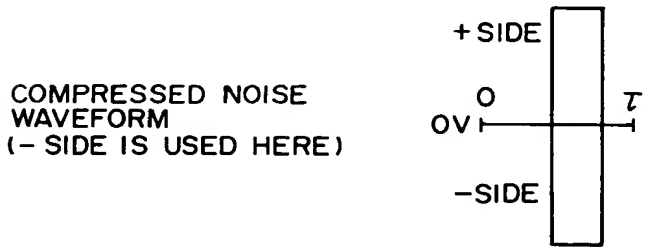


FIG. 40A

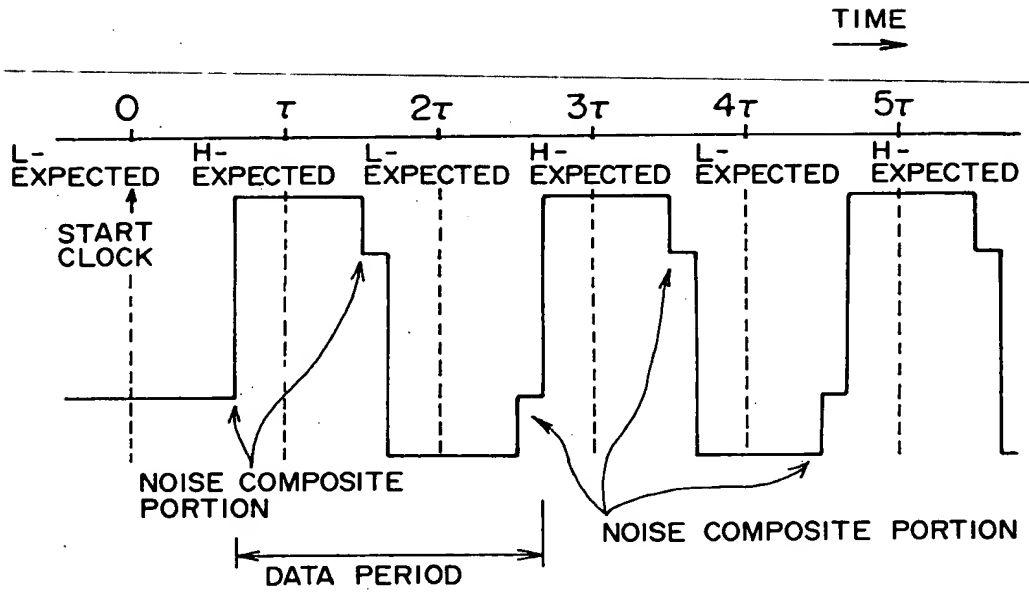


FIG. 40B

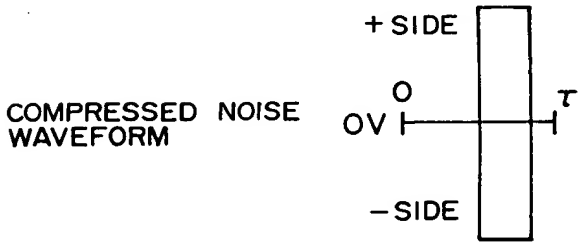


FIG. 41

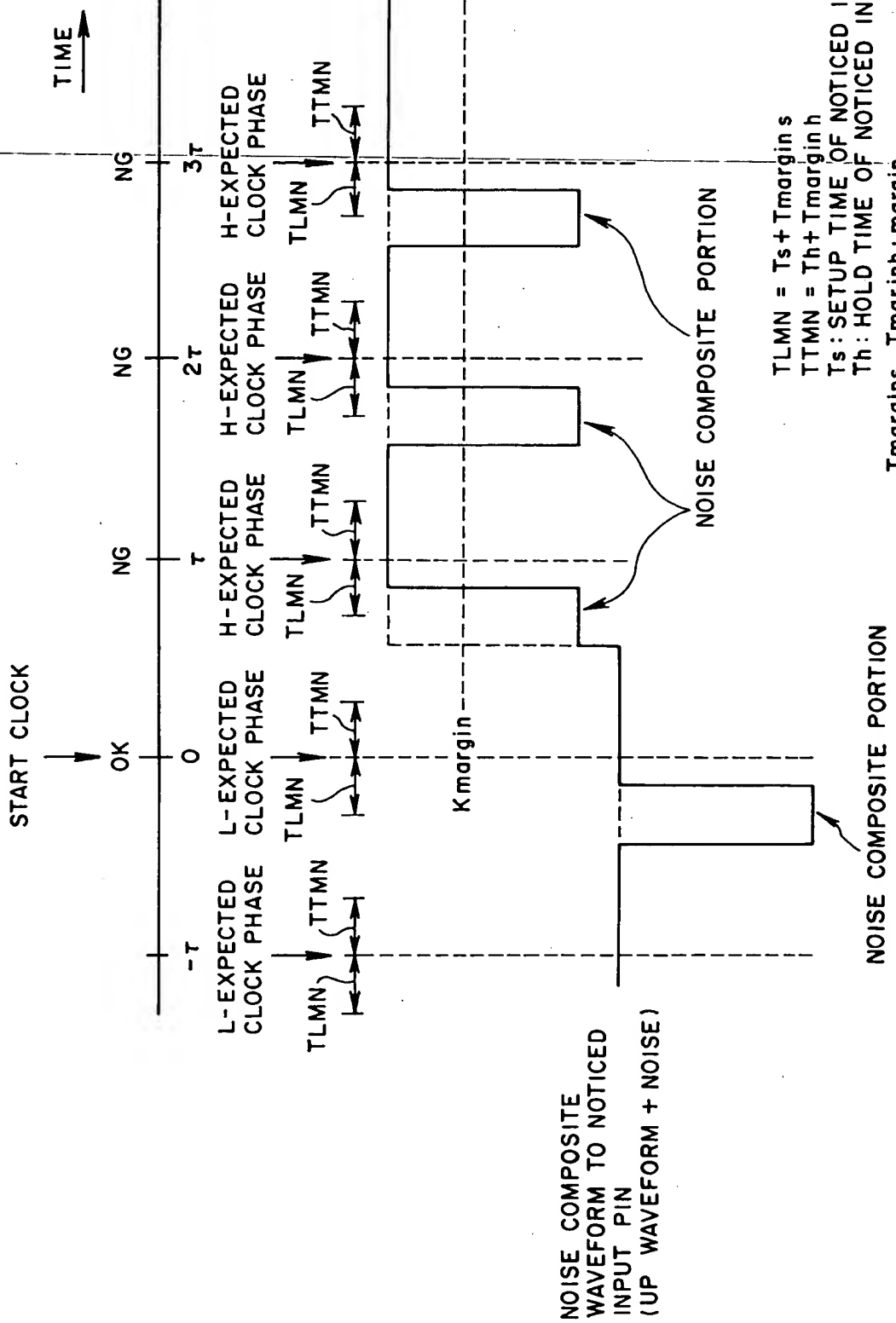

TIME
START CLOCK
OK
NG
NG
NG
-τ
0
τ
2τ
3τ
L-EXPECTED CLOCK PHASE
L-EXPECTED CLOCK PHASE
H-EXPECTED CLOCK PHASE
H-EXPECTED CLOCK PHASE
H-EXPECTED CLOCK PHASE
TLMN
TTMN
Kmargin
NOISE COMPOSITE PORTION
NOISE COMPOSITE PORTION
NOISE COMPOSITE WAVEFORM TO NOTICED INPUT PIN (UP WAVEFORM + NOISE)
TLMN = Ts + Tmargin s
TTMN = Th + Tmargin h
Ts : SETUP TIME OF NOTICED INPUT PIN
Th : HOLD TIME OF NOTICED INPUT PIN
Tmargins , Tmarinh : margin

FIG. 42A

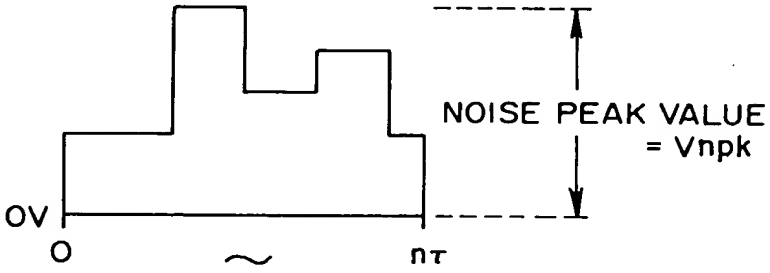


FIG. 42B